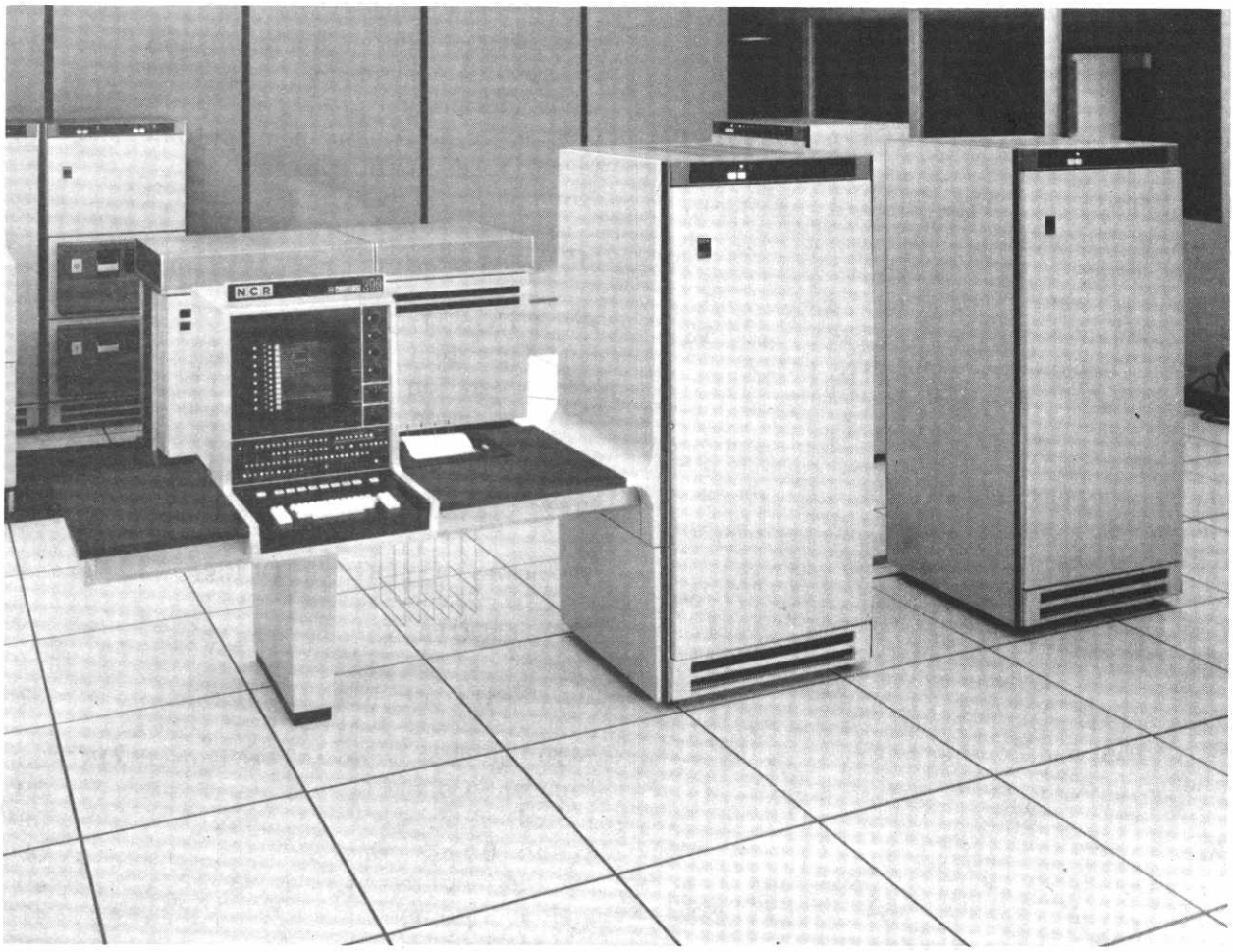
NCR CENTURY 300 PROCESSOR



This publication contains the functional description of the NCR Century 300. The General Introduction highlights the features of the NCR Century 300, while subsequent chapters (Memory, Arithmetic Logic Processor, I/O Control, and Operator's Console) cover these features and their related functions in more detail.

This functional description is not intended as a reference manual for programming and operating the NCR Century 300.

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GENERAL INTRODUCTION

The NCR Century 300, a medium- to large-scale data processing system, offers increased data-handling capabilities and improved cost/performance ratio through its ability to consolidate a number of applications into a single multiprogramming environment. Advanced operating systems and special hardware features permit the NCR Century 300 to control large online systems using many remote terminals, while running several batch (background) programs simultaneously. A full set of decimal and floating point arithmetic commands makes the NCR Century 300 equally powerful in both business and scientific applications.

Higher internal speeds, higher I/O speeds, and increased memory speeds, provide a total system throughput manyfold that of the smaller NCR Century systems. Availability to the user is increased through greater reliability and maintainability.

The 71 hardware commands of the NCR Century 300 include all the commands of the smaller NCR Century processors. Commands such as decimal multiply and divide, table compare, logic, scan, floating point arithmetic, and word commands, along with features such as multiprogramming and trace with monitor are standard on the NCR Century 300. In keeping with the NCR Century philosophy of upward compatibility, programs compiled on smaller NCR Century systems may be run on the NCR Century 300, without recompilation.

NOTE

> To take full advantage of the increased capabilities of the NCR Century 300 processor and to realize the savings in time and the gains in throughput, it is recommended that programs be recompiled on the NCR Century 300.

SYSTEM ORGANIZATION

For increased information processing capabilities and speed, the NCR Century 300 system utilizes the latest technological developments and advances in hardware design and construction: data is processed a word (4 bytes) at a time; memory is accessed to read or write data a word at a time; multiple processing elements are used to perform instruction setup, arithmetic and logical functions, and data input-output concurrently.

The NCR Century 300 system consists of Memory, Arithmetic Logic Processor (ALP), Input-Output Control (IOC), common trunk facilities for a wide array of peripherals, and certain integrated peripherals for communicating with and controlling the system.

Data is stored in a random-, direct-access memory, which may range in size from a minimum of 128K to a maximum of 4096K (K = 1024 bytes).

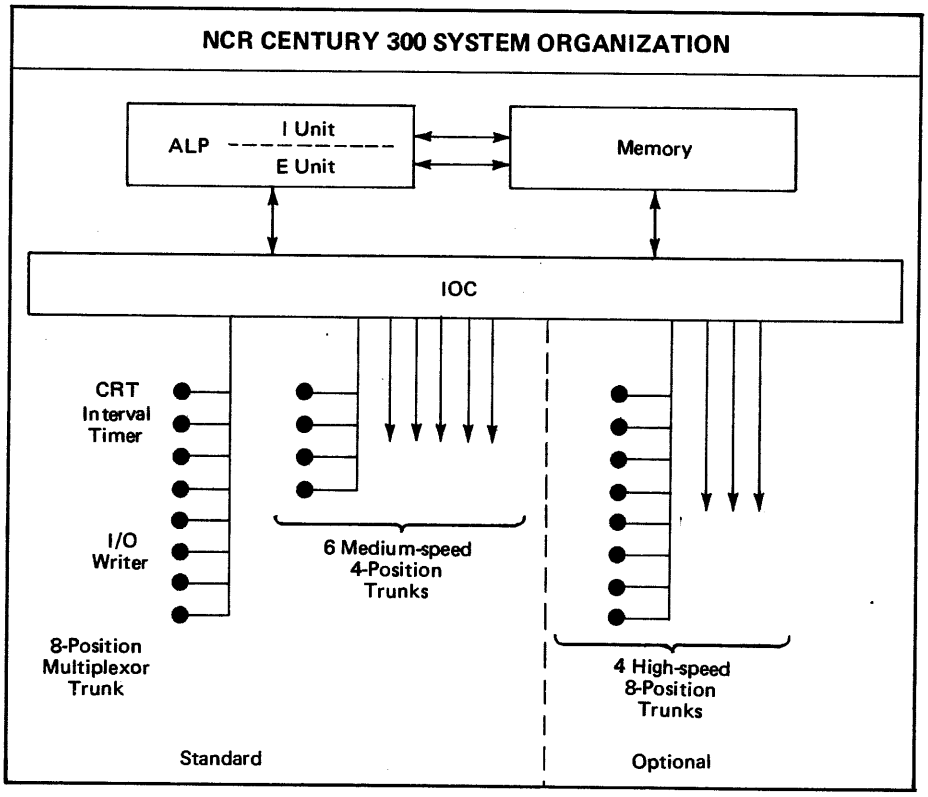
The ALP is a high-speed information processing device, consisting of two distinct units: the instruction setup unit (I unit) and the instruction execution unit (E unit). Each unit has separate access paths to memory and operates independently of and simultaneously with the other.

The IOC is an independent data input-output processor that controls and regulates all data flow between the peripherals and memory and performs other associated logic functions. The IOC has an independent, separate access path to memory.

The common trunks are data input-output channels that connect the peripherals to the IOC. The common trunks consist of an 8-position multiplexor trunk, six 4-position medium-speed trunks, and four optional 8-position high-speed trunks.

The integrated peripherals used for communications and control are the Thermal I/O Writer, the Interval Timer, and the CRT Display Unit.

The following illustration is a diagram of the NCR Century 300 system organization.



MEMORY

Data is stored in memory storage units (MSUs) whose capacities may be 128K, 256K, 384K, or 512K. Minimum memory size is 128K; maximum is 4096K. A maximum of eight MSUs may be used in a system, in any combination of storage capacities, within the limitations defined in "MSU Configurations," under "MEMORY ORGANIZATION," in the MEMORY chapter of this publication.

Data is represented internally in the 8-bit ASCII code. Besides the internal code, data may be represented as pure binary or binary-coded-decimal (BCD) numbers. Data fields are variable and data is byte-addressable.

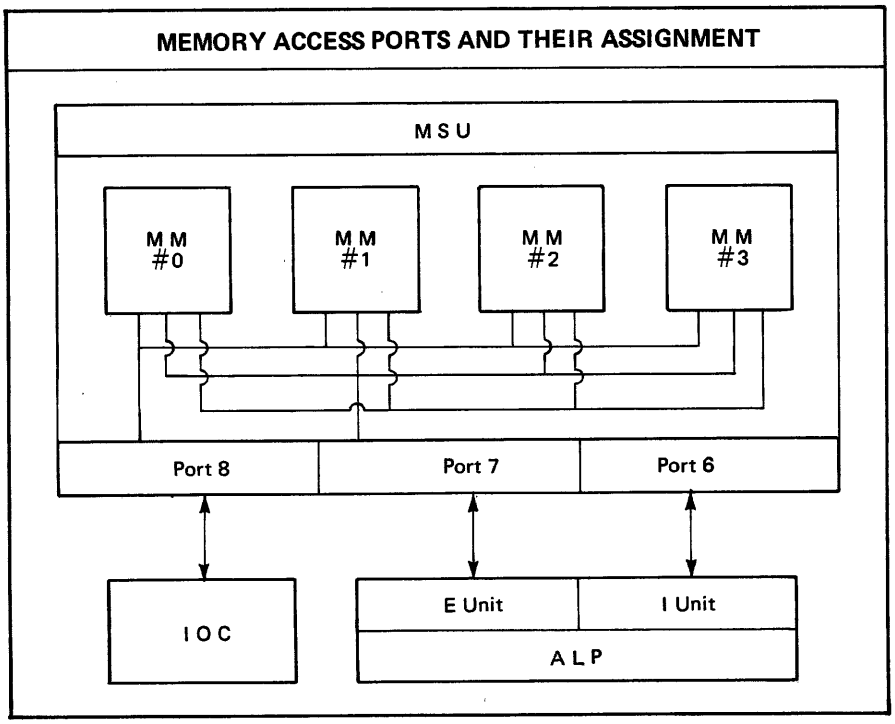
Information processing occurs a word (4 bytes) at a time, with data storage and retrieval occurring also a word at a time. Word processing and storage increase memory throughput, in comparison to character processing, four times. Memory address interleaving, explained later in this publication, further speeds up the total data storage and retrieval times.

Each MSU contains four memory modules (MM). Depending on the total storage capacity of the MSU, the MM capacity may be 32K, 64K, 96K, or 128K. Each MM is an independent unit and contains the necessary logic and timing circuits tc cycle simultaneously with any of the others.

Memory Access Ports

Data transfer between memory and accessing units is through interfacing logic, called memory ports, in the MSU. Each accessing unit (IOC, E unit, I unit) is assigned an access port to memory. By having individual access ports, an accessing unit is able to initiate a memory cycle in an MM while a cycle is still in progress in another MM. With independent memory ports, as many as three MMs in an MSU may be cycling simultaneously, each one having been initiated by a different unit. This reduces the access contention time, thereby increasing the effective memory access speed. If two units request access to the same MM at the same time, preassigned port priority determines the sequence of access.

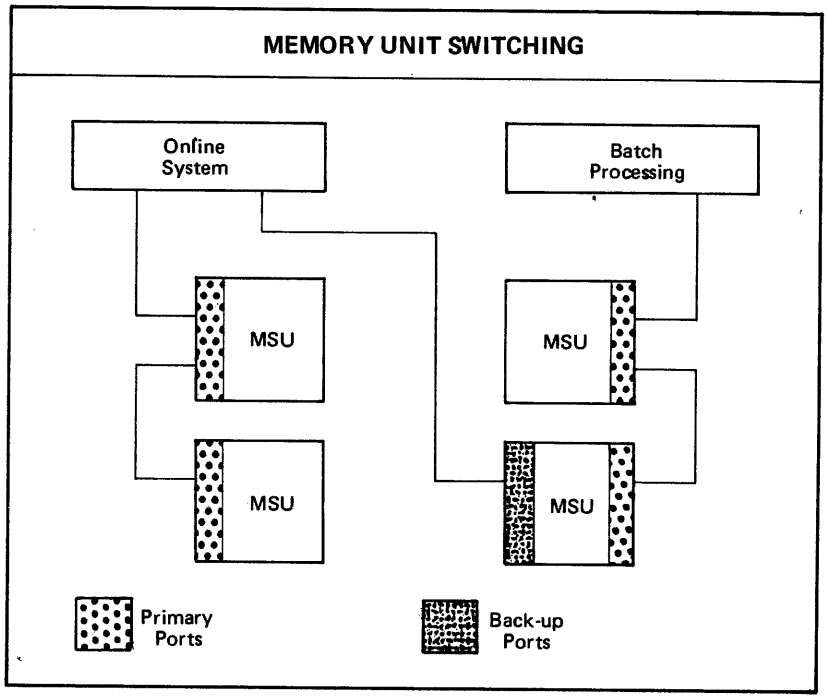
The following illustration shows the memory port assignment to the accessing units and the internal connections to the individual memory modules.



Memory Unit Switching

Each MSU is equipped with three memory ports, one each for the IOC, the E unit and the I unit of the ALP. If conditions warrant, the MSU may be equipped with three or six additional ports, as an option. In addition to the three accessing units mentioned above, a direct access device such as an emulator may be connected to the MSU. To facilitate connection of the direct access device, three optional ports may be added. In certain applications a dual system may be used, one serving online, the other processing batch programs. To keep the online system operating at full capacity, if one of the MSUs in the system fails, an MSU in the batch processing system may be switched to the online system. The disabled MSU is switched offline to the test mode, and the batch processing system is operated with reduced memory in a degraded capacity until the disabled MSU becomes operational. The ports are activated by the memory port enable switches on the MSU, so switching memory units becomes a relatively simple matter of disabling the access ports for one system and enabling the ports for the other.

The following illustration shows how the MSU of one system may be connected to serve as back-up unit for another system.

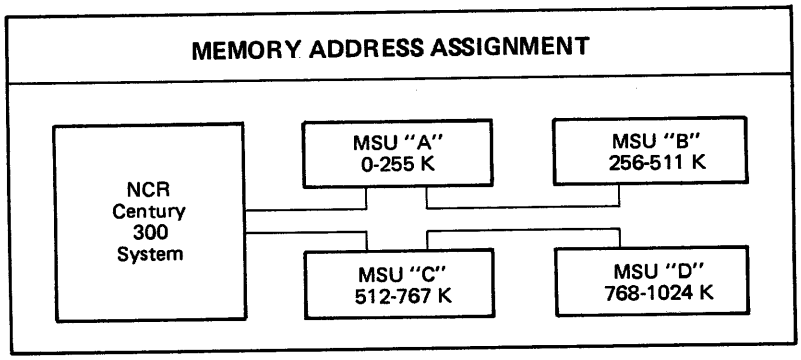


Memory Addressing

Memory addressing is performed by setting manual address assignment switches to the desired address range setting on the control panel of each MSU. Memory addresses are contiguous, beginning at the setting of the beginning address switch and continuing through the address range of the MSU according to its capacity. The next MSU beginning address switch is set to the next higher block of addresses, and so on until all available memory is assigned into blocks of contiguous addresses. Assigning blocks of addresses to the MSU by the address assignment switches lights up the corresponding memory ready lights

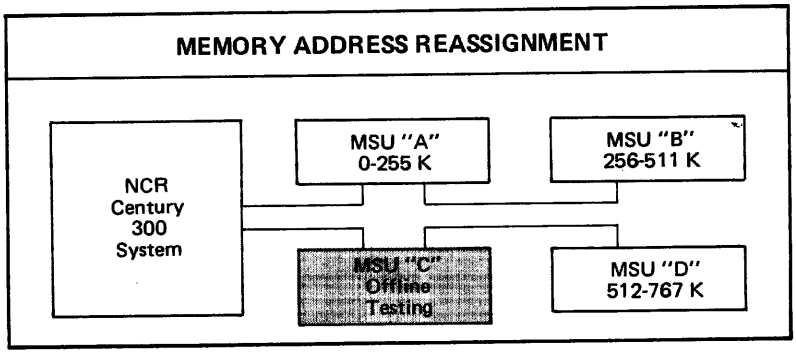
on the operator's console. Because the addresses are assignable by the operating personnel of the computer installation, the addressing scheme allows memory units to be switched in the system during the operating day if one of the MSU's should become inoperable. If an MSU, with a block of addresses within the total address range, becomes inoperative, the MSU with the highest address range may be reassigned to fill the address range of the inoperative MSU, while it is functionally taken out of the system and switched offline to the test mode for testing and corrective action.

In the following illustration, a total memory configuration of 1024K, in 256K units, has been assigned to operate within the shown address range.



During the operation, memory unit C becomes inoperative. Since an MSU may be assigned to operate within any range of addresses, the unit with the highest address block, unit D, is reassigned to operate within the address range formerly assigned to unit C. Although some degradation results because of the reduced memory, the system remains operational. The inoperative unit is switched offline for testing and corrective action.

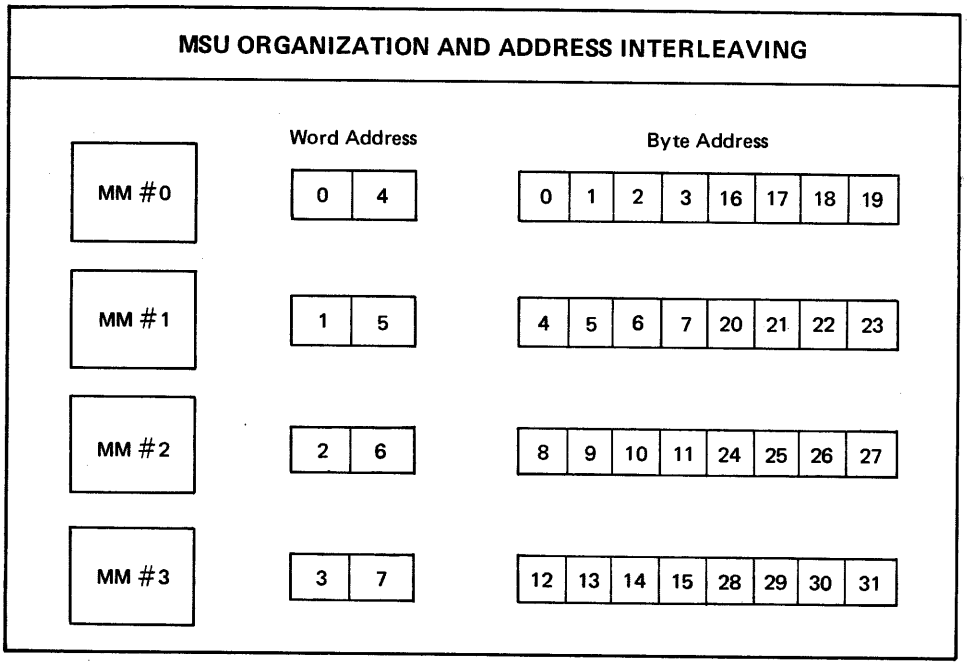
In the following illustration, the addresses have been reassigned, and the faulty unit, MSU C, is shown in offline testing.



Memory Address Interleaving

Memory address interleaving is a concept of addressing where data words corresponding to consecutive addresses are in different modules and can be accessed simultaneously. Each memory module contains data words whose addresses are multiples of four; that is, word 0, stored in memory module 0, is followed by word 1, stored in memory module 1, and so on. The next word stored in memory module 0 would be word 4, then word 8, and so on.

The following illustration shows the organization of an MSU and the relationship of word addresses to byte addresses.



Optional Time of Day Clock (TOD)

The control memory portion (0 - 128K) of the system usually contains the optional Time-of-Day Clock (TOD). The inclusion of the TOD is required by the operating system. The TOD is a free-running register whose output, when accessed by software, is decoded to give the actual time in hours and minutes. The clock is used for time-stamping messages displayed to the operator, timing program runs, entries in the error log, and other time-dependent functions of the system.

ARITHMETIC LOGIC PROCESSOR (ALP)

Three main features in the ALP substantially increase the internal processing speed and throughput of the processor: word processing, asynchronous operation, and E and I unit simultaneity.

Word processing increases the data throughput by a factor of four, when compared to processors that perform byte processing. By performing arithmetic and logic functions with four bytes, multiple memory accesses are eliminated and time-consuming housekeeping functions are reduced to a minimum. The result is more data processed in less time.

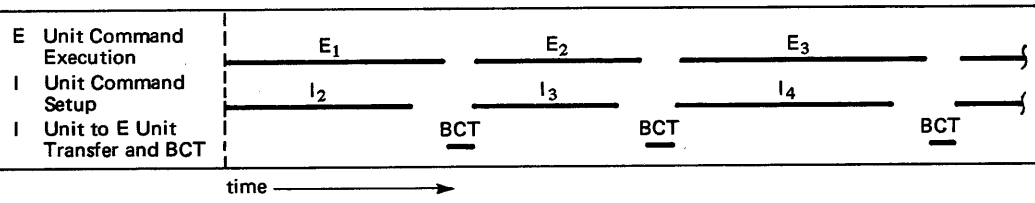
Asynchronous operation means that each unit (E and I unit) operates without an external clocking scheme, independently of and simultaneously with the other. Since each unit provides its own sequencing through an internal clock, the processor cycles of each unit are variable, determined by the operation being performed. Because of faster internal speeds, processor cycles are approximately one third of the memory cycle duration.

E and I Unit Simultaneity

The division of the ALP into two functional units, the instruction setup unit (I unit) and the instruction execution unit (E unit), results in simultaneous operations, where one unit is setting up a command while the other unit is executing a previously set up command. Each unit operates asynchronously of the other. The two units are synchronized only during the time the I unit transfers the set up command to the E unit for execution. During that time, checking for interrupt conditions, transfer-of-control conditions, and extensive error checking, known as Between-Command Testing (BCT), takes place.

The following illustration shows the time relationship between the operation of the I unit, the E unit, and the BCT functions.

TIME RELATIONSHIP OF E AND I UNIT OPERATIONS



E_1 = Execution of command 1, set up previously by the I unit.

I_2 = Setup of command 2, performed simultaneously with E_1.

BCT = I unit to E unit transfer and Between-Commands Testing.

E_2 = Execution of command 2, set up during the execution of command 1.

I_3 = Setup of command 3, performed simultaneously with E_2.

BCT = I unit to E unit transfer and Between-Commands Testing.

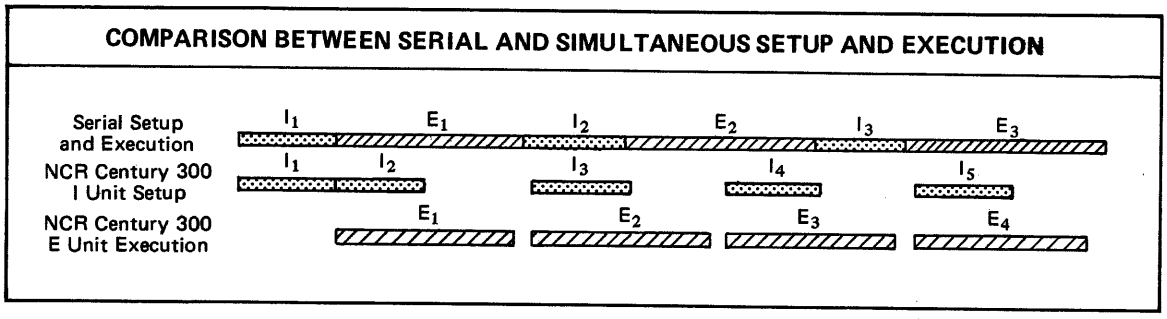
E_3 = Execution of command 3, set up during the execution of command 2.

I_4 = Setup of command 4, performed simultaneously with E_3.

BCT = I unit to E unit transfer and Between-Commands Testing.

In the majority of cases, the operation of the E unit and the I unit is simultaneous during the running of the program. Exceptions are the indirect addressing, incremental indexing, or the sequential setup stages by the I unit. Before the I unit can complete these setup stages, the E unit must have terminated the execution phase of the previous command.

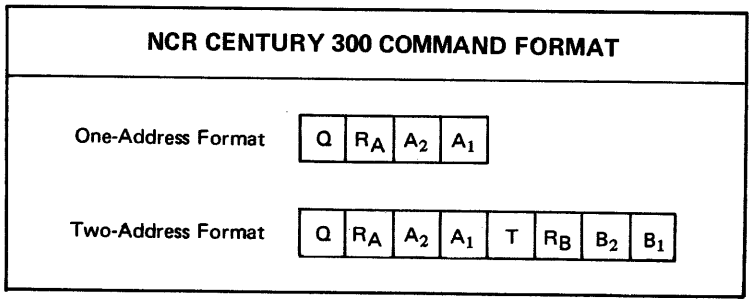
The simultaneous setup and execution mode of operation results in considerable time-savings when compared to the serial setup and execution mode of other systems. The following illustration demonstrates graphically the increased speed obtained by the simultaneous operation of the I and E units when compared to the serial operation of these units.



Command Format

The commands stored in memory are either in a one-address format (four bytes) or a two-address format (eight bytes).

The following illustration shows the one-address and the two-address command formats, followed by definitions of each byte in the command.



Q -- Command code, the operating instruction to the processor.
RA -- Specifies mode of addressing, indexing, and the index register number used.
A2A1 -- The partial address of the A operand. If the partial address is not modified, then the contents of bytes A2A1 becomes the effective A operand address.
T -- Field length of both A and B operands. (In some special commands, the T value specifies something other than field length. These exceptions are explained in the "NCR Century 251/300 Hardware Commands," under this tab.)
RB -- Same as RA, for the B operand.
B2B1 -- Same as A2A1, for the B operand.

In a one-address command, field length and B operand address are implied; that is, the T value used is the one set up by a previously executed two-address command, and the B value used is the contents of the B operand address register at the conclusion of the previous command execution.

Although data is byte-addressable, where the starting address may be any legal address in memory, the starting addresses of commands must be 0 modulo 4 (evenly divisible by four), or a Programming Error (PE) results.

Addressing Modes

Addressing may be performed in one of four modes: direct addressing, two modes of indirect addressing, and incremental indexing of addresses. A detailed description of addressing modes follows in the ARITHMETIC LOGIC PROCESSOR chapter of this publication, under the heading of "Instruction Format and Indexing."

Multiprogramming

Multiprogramming enables the processor to handle two or more programs simultaneously, thereby reducing the processor idle time, increasing the total processing capabilities, and reducing the total effective time required for running a certain number of programs. Program separation during multiprogramming is accomplished by multiple BAR (Beginning Address Register) and LAR (Limiting Address Register) registers which protect one program from accessing memory areas assigned to another. The use of BAR/LAR registers also simplifies programming by permitting all programs to start at relative memory location zero. Memory protection is provided by a Write Prohibit flag and a Segment Unavailable flag, used in conjunction with each BAR/LAR register.

Storage of index registers in memory, rather than hardware "live" registers, allows each program to have its own individual set of 63 index registers. This reduces software overhead considerably, since the contents of the index registers do not have to be saved each time program switching occurs. The memory-resident index registers also eliminate the need for a number of hardware commands for register manipulation.

Hardware Commands

The common trunk feature, using only one I/O command for initiating all data input-output functions, eliminates the need for several I/O hardware commands. By also eliminating a number of commands for register manipulation, only 71 hardware commands are needed to control the extensive information processing capabilities of the NCR Century 300 system.

The following list contains the commands of the NCR Century 300, in groupings of their major functions:

- 11 Fixed Point Binary Commands
- 12 Floating Point Commands
- 9 Decimal Arithmetic Commands
- 3 Move Data Commands
- 8 Logical Commands
- 13 Transfer Commands
- 15 Special Commands

INPUT-OUTPUT CONTROL (IOC)

The input-output operations of the NCR Century 300 work on the common trunk concept, compatible with all NCR Century Series Processing Systems. The common trunk concept, simplified, means that all peripherals interface with the I/O trunk in a like manner, which permits the use of a single I/O command.

Separation of data lines from the control lines, in the common trunk, permits the simultaneous selection of like peripherals, working under the supervision of one control unit. For instance, a disc controller, controlling eight disc units, may issue "seek" instructions to seven units while transferring data from an eighth unit. All units performing the seek function do so simultaneously, without any detrimental effects on the data transfer.

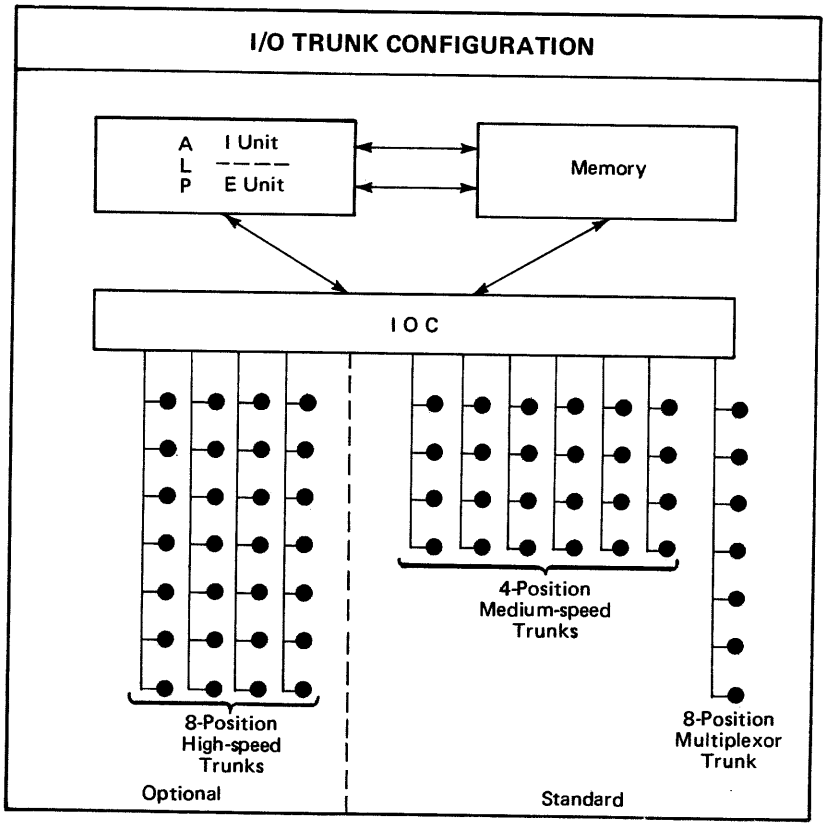
To detect errors in transmission and other hardware malfunctions, and to verify the correctness of the transmitted information, all control characters (selection, data-request, terminate, etc.) and all data characters (information) are transmitted with a parity bit. The parity bit is generated by the sending unit and checked by the receiving unit. Use of parity during the I/O operation increases system reliability by protecting data integrity and preventing selection of the wrong peripheral.

Trunk Configuration

Two possible I/O trunk configurations are available with the NCR Century 300: the standard and the optional.

In the standard I/O trunk configuration, with six 4-position medium-speed trunks and an 8-position multiplexor trunk connected to the IOC, 14-way I/O simultaneity is possible. In the optional I/O trunk configuration, with four 8-position high-speed trunks added to the standard configuration, 18-way I/O simultaneity is possible.

The following illustration is a diagram of the I/O trunk configuration of the NCR Century 300 system.



Peripheral Unit Selection

The processor initiates an I/O operation by executing an I/O command. The I/O command specifies a memory location that contains the desired Peripheral Address Field (PAF).

The PAF specifies the trunk number, the position number on the trunk, a function code (read, write, rewind, etc.), and other pertinent data, depending on the peripheral unit to be selected (for instance, cylinder, head, and sector number, if a disc is selected). When the peripheral unit has received the necessary information, it sends an End-of-Control-Information (ECI) signal to the processor, which terminates the I/O command. The processor proceeds to the next command in sequence. The actual data transfer is under the supervision of the IOC.

Data Transfer

The selected peripheral readies itself for data transfer at the completion of the selection process. When the peripheral is ready to receive or transmit data, it notifies the IOC by sending it a service-request signal. The IOC responds by sending the peripheral a start signal and the data transfer commences to or from the peripheral.

Each 4-position trunk is assigned a "live" control word and a "live" 1-word buffer in the IOC. This reduces the memory accesses for address incrementation in the control word, and for data retrieval and putaway. Since the IOC has its own access port to memory, data putaway is accomplished one word (four bytes) at a time, as the buffers become filled. Similarly, when outputting data to a peripheral unit, a word is read from memory and stored in the appropriate buffer in the IOC. From this buffer, the data is transmitted to the peripheral unit one byte at a time, until the buffer is emptied. Memory is then accessed again for the next word.

Positions 0, 1, and 5 of the multiplexor trunk are dedicated to the CRT Display, the Interval Timer, and the I/O Writer, respectively. Since all positions on the multiplexor trunk can be active at the same time, "live" buffers and control words are not used. Instead, an 8-position scanner checks each position of the trunk for activity and stores the data directly in memory, a byte at a time, as it is received. For online communications with remote terminals, the NCR 621 Multiplexor, with selfcontained control logic and sequencing, can accommodate up to 253 communication lines. The Multiplexor may occupy any of the non-dedicated positions on the multiplexor trunk.

With the expanded, optional I/O trunk configuration, the four optional 8-position high-speed trunks, like the standard trunks, have a "live" control word for each trunk. The buffers, however, have been increased to two words per trunk, for more efficient data transfer with high-speed peripherals.

Data Transfer Rates

Data transfer rates depend on many different factors: memory speed, the number of trunks operating simultaneously, the transfer rate of the various peripheral units in operation, and the physical location (cable length) of the connected units. The maximum I/O transfer rate of the NCR Century 300 system is 3.7

megabytes per second. Operating at the maximum I/O rate, there is minimal degradation in the compute rate of the ALP.

The following table lists the trunk transfer rates and the system I/O bandwidth of the NCR Century 300.

SYSTEM I/O BANDWIDTH AND TRUNK TRANSFER RATES

I/O Configuration	System I/O Bandwidth	Trunk Transfer Rates		
		4-Position Trunks	8-Position Trunks	Multiplexor Trunk*
Standard	2740 KB	815 KB	–	120 KB
Optional	3720 KB	815 KB	1040 KB	120 KB

* The data transfer rate of the Multiplexor trunk varies, depending on the number of active positions on the trunk. For a detailed description of multiplexor trunk transfer rates, refer to the INPUT-OUTPUT CONTROL chapter of this publication.

I/O Termination

I/O termination results when an I/O operation is completed. (All terminating conditions are covered in detail in the INPUT-OUTPUT CONTROL chapter of this publication, under the heading "Termination.")

For the efficient handling of I/O terminations, each I/O function is assigned a priority level. Each program being executed in the ALP is also assigned a priority level. The priority levels range from 0 through 15. If the I/O function has a higher priority than the program being executed at the time, the program is interrupted and the I/O termination is serviced. If the program, however, has a higher priority than the terminating I/O function, no interruption occurs. Instead, the IOC makes an entry in a termination queue table and sets a flag in a queue pointer list to indicate that an I/O operation terminated. When the next program interrupt occurs, the termination is serviced.

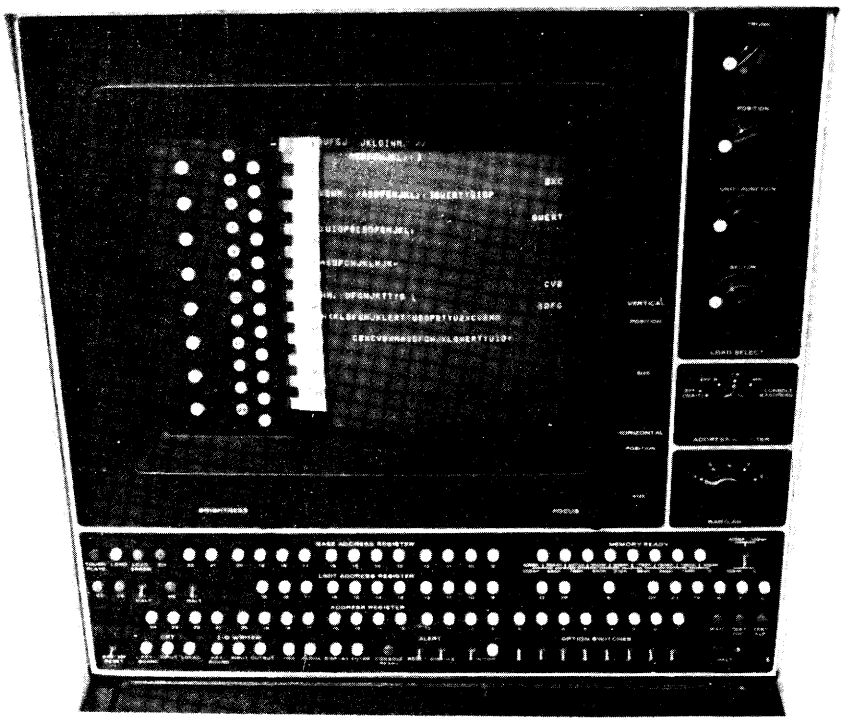
The use of termination queues and queue pointers eliminates the necessity of the processor having to interrupt its program flow and enter the I/O termination routine every time an I/O termination occurs. This minimizes software overhead, by allowing I/O terminations to be processed selectively, according to priority. The establishment of interrupt priorities also prevents relatively low-priority I/O terminations from interrupting a high-priority program that is active at the time.

OPERATOR'S CONSOLE

The Operator's Console, consisting of a CRT Display Unit, an I/O Writer, a Control Panel, and a keyboard shared by the CRT Display Unit and the I/O Writer, is the communications and control center of the NCR Century 300. The console, an integral part of the processing system, enables the operator to make full use of the extended operating systems, and increased hardware capabilities of the NCR Century 300.

The primary means of communications between the operator and the computer is the CRT Display Unit, whose functional capabilities are dependent, to a large degree, on the operating system under which the computer is operating. Generally, the operator is provided the means to access program and system status and related information, as well as to enter instructions and information through the keyboard. For a detailed description of operator communications, refer to the NCR CENTURY OPERATORS INFORMATION MANUAL.

CRT DISPLAY AND TOUCHPLATE SWITCHES



System software uses the CRT Display Unit to display the system status. The system status display is organized in an expanding, tree-like, hierarchical structure. The operator, by pressing the touchplate switches corresponding to the lines, may access any level of the tree-like structure. Information concerning peripheral availability, peripheral status, job queueing, or the list of pending messages is immediately available to the operator, as shown on the following illustration.

The CRT Display Unit includes 32 touchplate switches: 24 numeric switches which are aligned with the corresponding lines on the screen, and 8 alpha control switches, placed immediately to the left of the line switches.

Some of the numeric switches display the entry on the corresponding line on the CRT. They are used with the System Display messages to the operator, such as current jobs, pending jobs, etc. Others request a display of pending messages from the system or the user.

The alpha control switches are used to place the DISPLAY INDEX on the CRT screen, to display the next higher level of the display hierarchy, or to print a hard copy of the current CRT display on the I/O Writer. Certain displays may overflow the CRT screen. In such cases, the display is split into two or more pages. The multi-page display can be viewed by using control switches to "page forward" or "page backward."

SYSTEM AVAILABILITY

Higher cost of computers and the ever-increasing trend toward online realtime applications necessitates greater reliability of computers and increased availability to users. Availability is directly dependent on the reliability and the maintainability of the product.

The NCR Century 300 is designed, from the selection of hardware components through final testing to meet rigorous quality control standards, to provide a high degree of reliability.

Since reliability, after completion of the manufacturing process, becomes a fixed factor, availability is affected primarily by maintainability. To increase the availability of the equipment to the customer, the NCR Century 300 incorporates extensive aids in dynamic fault isolation, as well as offline testing facilities, to improve maintainability.

Diagnostic Aids and Testing Facilities

The diagnostic capabilities of the NCR Century 300 are arranged in three levels of comprehensiveness and operation:

1. Detection and logging of malfunctions to aid the technical representative in detecting patterns or trends in the occurrence of these malfunctions. This log is valuable in isolating highly intermittent faults and faults that are not system-disabling.

2. Diagnostic programs, written in a more elementary machine language that uses microdiagnostic hardware (nonprogrammable wired-in logic), are used to isolate faults in the ALP and the IOC where extensive testing at internal computer speeds is required. Microdiagnostics are extremely valuable in establishing the integrity of the basic processing system (ALP-IOC).

3. Comprehensive test panels are included in individual units (ALP, IOC, MSU, and peripherals) for effective offline testing and trouble-shooting in the occurrence of semi-solid, solid, or predictable faults.

MEMORY

INTRODUCTION

The NCR Century 300 features expandable data storage capacities from a minimum of 128K to a maximum of 4096K (K = 1024 bytes) of core memory.

Memory is organized into Memory Storage Units (MSU) which may vary in total capacity from 128K to 512K. The system may have a maximum of 8 MSUs. Each MSU is housed in a standard high-boy cabinet, 66 inches high, 32 inches wide, and 27 inches deep.

Each MSU contains 4 Memory Modules (MM) which may vary in total capacity from 32K to 128K each. The capacity of the individual MMs determines the capacity of the MSU.

The basic data storage grouping is a 40-bit word. The 40-bit word is made up of 32 data bits, with the remaining eight used for error checking.

Although data is read from, or written into, memory a word (4 bytes) at a time, to be compatible with the processing units, the ability to address data by byte is maintained. The processing units have the logical capability to initiate read or write of partial words by blocking specified bytes from being transferred to or from memory.

Each processing unit (IOC, E unit, I unit) has a separate, independent access path to memory. Each MM is capable of cycling independently of the others. These two features make possible simultaneous accesses by the processing units, each accessing and cycling a different MM at the same time. The simultaneity of operation (memory accesses) results in increased memory throughput and increased efficiency of the system.

DATA REPRESENTATION

The 8 bits in a byte may be used to represent two packed binary coded decimal (BCD) numbers, 8-bit binary numbers, or 8-bit NCR Century characters (4 zone bits and 4 digit bits).

NCR CENTURY CODE CHART

B_8-B_5 \ B_4-B_1		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL	SOH	STX	ETX	EOT	ENQ	ACK	BEL	BS	HT	LF	VT	FF	CR	SO	SI
0001	1	DLE	DC1	DC2	DC3	DC4	NAK	SYN	ETB	CAN	EM	SUB	ESC	FS	GS	RS	US
0010	2	SP	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0011	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
0100	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
0101	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
0110	6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
0111	7	p	q	r	s	t	u	v	w	x	y	z	{	¦	}	~	DEL

Note that in the code chart b8 is always 0, limiting the number of possible characters to 128. This configuration conforms to the American Standard Code for Information Interchange (ASCII).

Examples of Data Representation

b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	1	0	1	0	1	1	0

If the bit configuration above is considered as two 4-bit BCD numbers, the decimal values are 5 and 6.

8	4	2	1	8	4	2	1
0	1	0	1	0	1	1	0
	5				6		

If the same bit configuration is considered as a single, 8-bit binary number, the decimal value is 86.

128	64	32	16	8	4	2	1
0	1	0	1	0	1	1	0
			86				

If the same bit configuration is considered as a character in the NCR Century code, it is equivalent to a V.

b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	1	0	1	0	1	1	0
	zone bits				digit bits		

Word Format

A word stored in memory consists of 40 bits. Of the 40, 36 bits are utilized, 32 for data and 4 for parity.

FEATURES

Features of the MSU in the NCR Century 300 system are classified as standard or optional. Standard features are common to all MSUs, while the optional features are incorporated in the MSU only when specified by the customer.

Standard Features

Modularity -- Modular units allow memory to expanded from 128K to 4096K.

Manual Address Assignment -- Each MSU may be assigned to operate in any address range within the range of the total memory capacity. Two Address Assignment Switches on the MSU control panel determine the range of addresses to which that MSU is assigned. Address assignment, and reassignment if necessary, is, therefore, simplified and can be done quickly, without delay or shutting down the entire system.

Memory Address Interleaving -- Provides lower effective access time by assigning consecutive words to successive MMs. Simultaneous accesses by the three processing units (IOC, E unit, I unit) is made possible by memory address interleaving.

Memory Test Logic -- Each MSU has built-in testing facilities for exercising and testing the unit offline. This feature improves maintainability, which in turn increases availability to the user.

Optional Features

MSU Expandability -- The basic 128K MSU may be expanded to 256K or 384K, or 512K.

Time of Day Clock (TOD) -- The TOD is a free-running 32-bit binary counter, counting in 25-microsecond intervals, with an accuracy of ± .01%. When accessed by the ALP, the output of the counter is decoded by software to give the actual time of day. Normally stored in the control portion (0 - 128K) of the system, the TOD is required by the operating software.

Back-Up Ports -- In addition to the three standard ports used in the MSU, on a dual-processing site (2 NCR Century 300 systems), three additional ports may be added as back-up ports; in this manner, the MSU may be connected to both systems. The ports for either system may be enabled, depending on the need for memory by the individual systems. If a direct memory access device, such as an emulator, is connected to the system, an additional three ports must be added, for a total of nine memory ports.

MEMORY ORGANIZATION

Total memory capacity ranges from a minimum of 128K to a maximum of 4096K (K = 1024 bytes). Memory is organized into Memory Storage Units (MSU), comprised of four Memory Modules (MM), where data is stored in 4-byte words, organized into groups of 40 bits (32 data bits and parity bits).

Memory Sizes

Because of the modularity of MSUs, any combination of MSUs may be used to make up the total memory configuration, as long as the number of MSUs does not exceed eight.

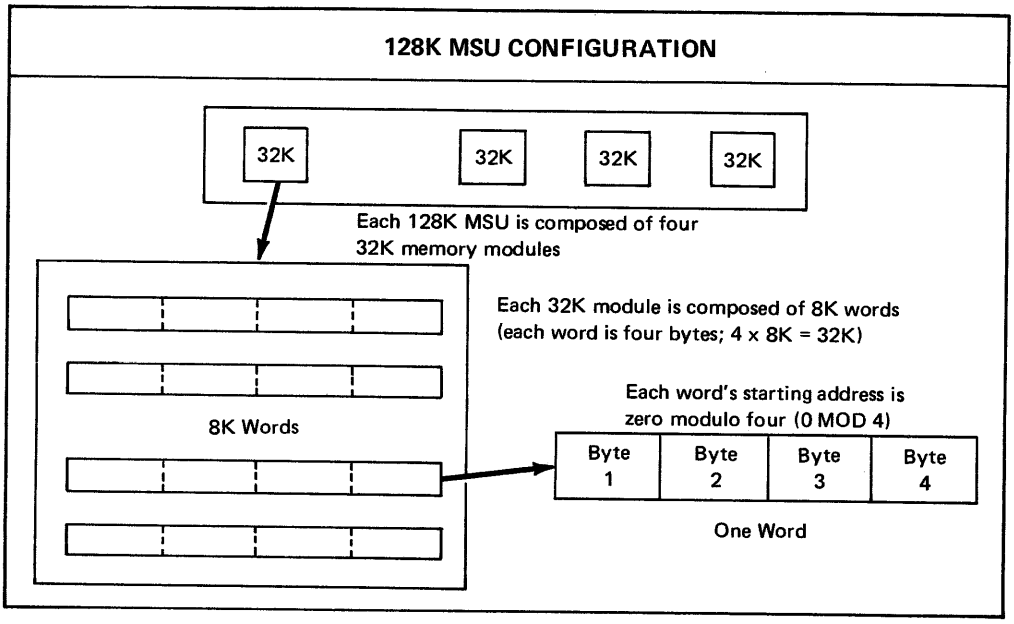
The following size memory configurations are available with the NCR Century 300:

128 K (131,072 bytes)	896 K (917,504 bytes)	2048 K (2,097,152 bytes)
256 K (262,144 bytes)	1024 K (1,048,576 bytes)	2560 K (2,621,440 bytes)
384 K (393,216 bytes)	1280 K (1,310,720 bytes)	3072 K (3,145,728 bytes)
512 K (524,288 bytes)	1536 K (1,572,864 bytes)	3584 K (3,670,016 bytes)
640 K (655,360 bytes)	1792 K (1,835,008 bytes)	4096 K (4,194,304 bytes)
768 K (786,432 bytes)		

MSU Configurations

Each MSU comprises four Memory Modules (MM). The MMs range in sizes of 32K, 64K, 96K, and 128K, making available four different capacity MSUs -- 128K, 256K, 384K, and 512K.

The following illustration shows the internal organization of a 128K MSU; the MMs are 32K each, with each MM having a storage capacity of 8K words (32K).



A maximum of 8 MSUs may be connected to the processing units, so the maximum memory capacity needed for the system determines the individual capacity of each MSU. Because of the limitation of eight maximum MSUs in a system, within the range of sizes shown in the folloiwng table, the MSUs may be only in certain increments.

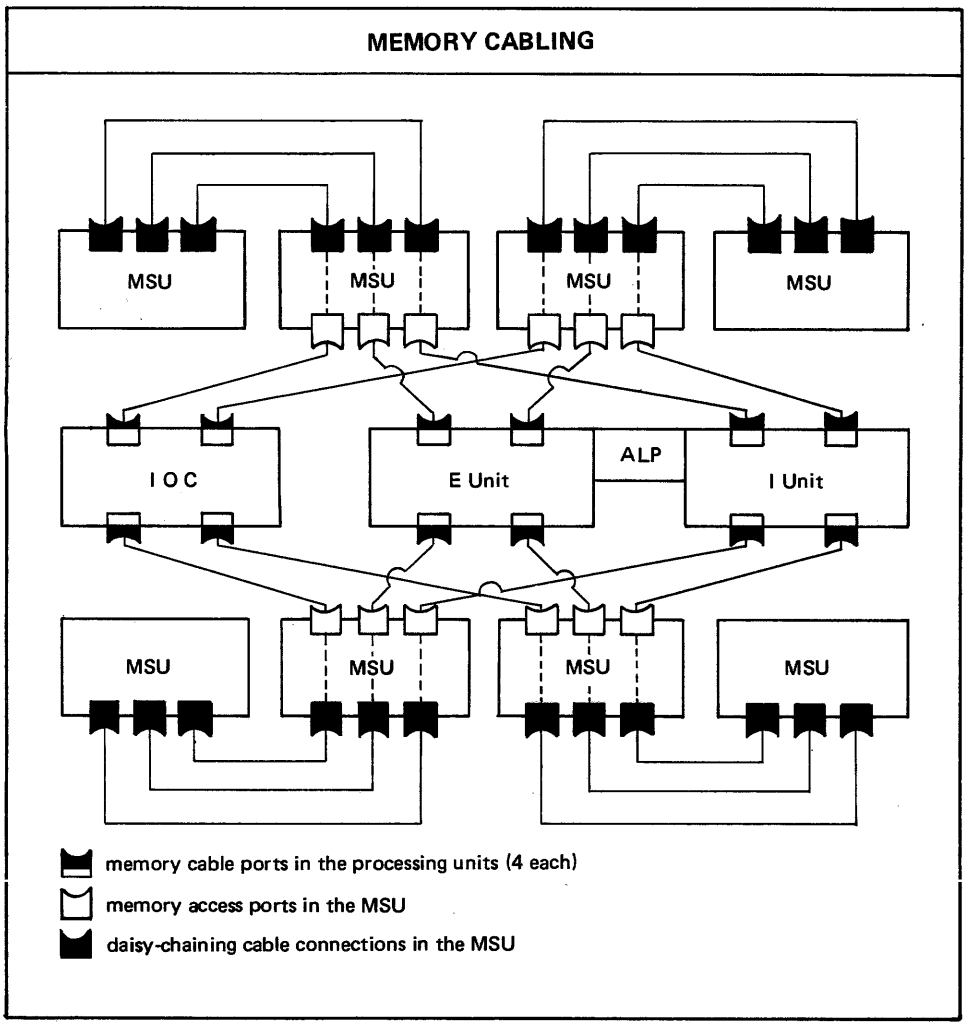
ALLOWABLE MSU SIZES WITHIN TOTAL MEMORY

Total Memory Range	Allowable MSU Size
0-1024K	128 K 256 K 384 K 512 K
1024K - 2048K	256 K 512 K
2048K - 4096K	512 K

Memory Cabling

Each processing unit (IOC, E unit, I unit) is equipped with four memory cable ports. Two MSUs may be daisy-chained, to allow the use of the maximum eight MSUs in a system. It is recommended that all cable ports in the processing unit be utilized before daisy-chaining MSUs. Maximum cable length between an MSU and a processing unit is 25 feet. (This includes the length of the cable used to daisy-chain two MSUs.)

The following illustration shows the diagram of memory cable connections between the processing units and the MSUs.



Memory Power Distribution

Port power to the memory port circuits is present whenever the main circuit breaker on the MSU is ON. Power ON and OFF Switches on the MSU control panel apply and remove AC in the MSU. Corresponding indicator lights are ON, whenever port or AC power is present.

Each MM contains its own power supply for core decode and drive circuits. A separate power supply provides DC power to the Memory Logic Panel and other common logic circuits.

AC power may be switched ON or OFF to an MSU without affecting other MSUs. However, if port power is lost at an MSU, all processing units connected to that MSU are rendered incapable of accessing any memory.

MEMORY ACCESS PORTS

The interfacing logic between the memory modules and the processing units is contained in the Memory Logic Panel (MLP) of the MSU. The cable connections to the MLP are referred to as memory ports.

Standard Ports

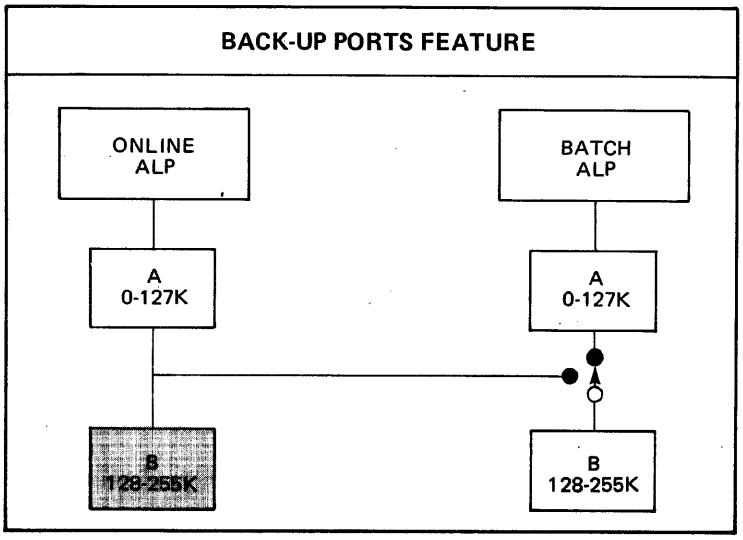
Each MSU is equipped with three standard memory ports, one each for the accessing units (IOC, E unit, I unit).

Optional Ports

If an MSU is connected in such a manner that it can be shared (switched from one to the other), for back-up purposes, by two processing systems, three ports may be added to the MSU, so it can be connected to both systems. Ports for only one system are enabled at a time.

If a direct memory access (DMA) device, such as an emulator, is connected to the MSU, three more ports are added to accommodate such a device.

The following illustration shows a dual processing system: one system is used for online processing, while the other is used primarily for batch processing.

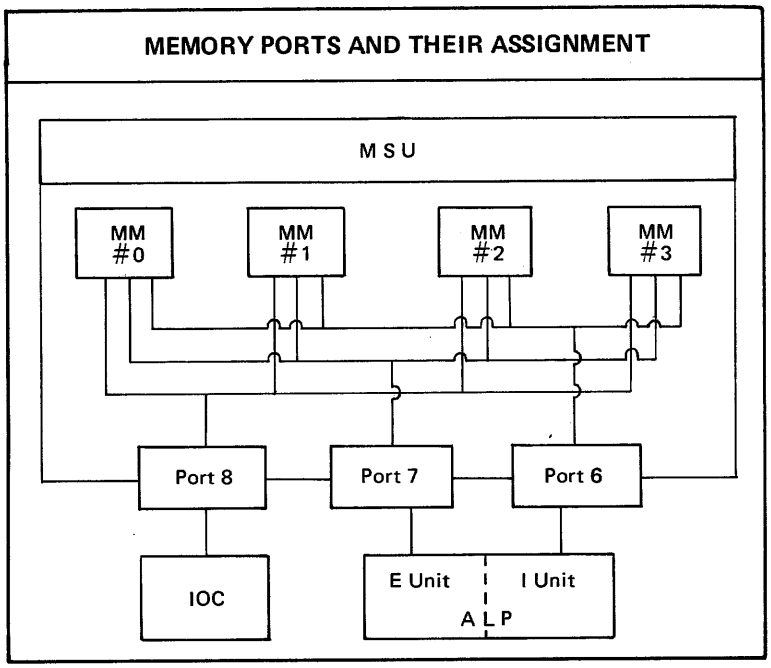


If memory unit B in the online system should become inoperative, one of the MSUs in the batch system can be switched to the online system manually. This keeps the online system "on the air" at full capacity. The batch processing system suffers some degradation because of the reduced memory storage, but it is still operational.

Port Priority

Port priorities range from 8 to 0, with 8 having the highest priority. Priority 8 is usually assigned to the IOC, with the next higher priority assigned to the E unit and then the I unit.

The following illustration shows memory access ports and their assignment in an MSU.



MEMORY ADDRESSING

Memory is not cyclic modulo physical memory size. Access to locations equal to or greater than physical memory size result in a Programming Error (PE).

Hexadecimal Address Representation

Binary addressing in NCR Century Systems keeps the need for hardware to a minimum. To facilitate the expression of binary addresses, NCR Century Systems use a hexadecimal representation of binary addresses.

Binary numbers are represented as hexadecimal values by dividing the binary field into groups of four bits. The value of each group of four bits is then expressed hexadecimally.

CONVERSION OF BINARY TO DECIMAL AND HEXADECIMAL VALUES

Binary	Decimal	Hexadecimal
0000	0	0
0001	1	1
0010	2	2
0011	3	3
0100	4	4
0101	5	5
0110	6	6
0111	7	7
1000	8	8
1001	9	9
1010	10	A
1011	11	B
1100	12	C
1101	13	D
1110	14	E
1111	15	F

Each group of four bits can range from 0 through 15 (decimally). The values are expressed hexadecimally as 0-9 and A-F. The following chart shows the conversion of 4-bit binary numbers to decimal values and to hexadecimal values.

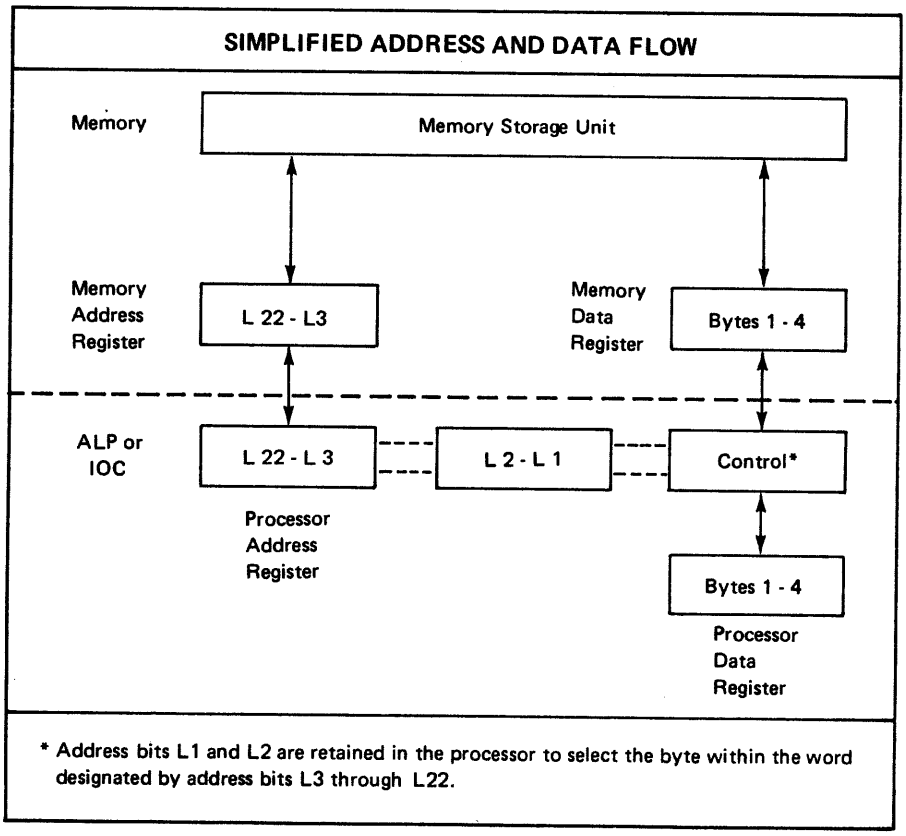
Address Bit Assignment

Memory addresses are contained in a 3-byte 24-bit binary address register. Only 22 of the 24 bits are used for address; bits 23 and 24 must be zeroes or a Programming Error (PE) results.

Of the 22 binary address bits, bits 1 and 2 are retained by the processing unit to designate the byte (bytes) that is (are) to be transferred and the byte (bytes) that is (are) to be suppressed. This allows data to be addressed by byte.

Bits 22 through 3 are the word address sent to the MSU. Of these, bits 22 through 18, in conjunction with the Address Assignment Switches (explained later), identify the MSU and the 128K, 256K, or 512K block of addresses within that MSU. Bits 3 and 4 with the Mode Select Switch (explained later, under Memory Address Interleaving) determine which of the four memory modules to select. Bits 17 through 5 determine the word location within that module.

The following illustration is a simplified chart of address and data flow between processor and memory.



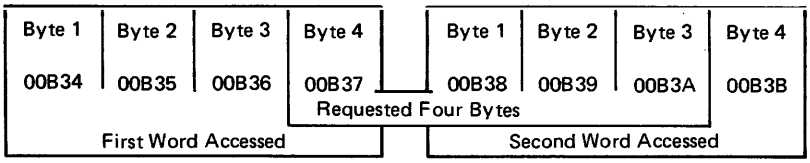
Byte Addressing

Although the starting addresses of data words are zero modulo four (0 mod 4), each byte within a word may be addressed individually due to the ability of the processing unit to block the transfer of the unrequested byte (bytes) to or from memory.

If the address of a requested byte is not zero modulo four, it is adjusted to the next lower address that is evenly divisible by four. Even though any byte or series of contiguous bytes can be accessed during a memory operation, the entire word (nearest lower zero modulo four address) that contains the requested byte is always accessed. All four bytes of an accessed word may or may not be required by the operation taking place.

In the following example, bytes 00B37, 00B38, 00B39 and 00B3A must be accessed for an operation.

The address of the most significant byte is 00B37. This byte is contained in the memory word addressed as 00B34, the next lower zero modulo four address. The word located at 00B34 is read from memory and stored in a data register. The memory addresses of the four bytes in the word are 00B34, 00B35, 00B36, and 00B37; byte 00B37, the requested byte, is saved, the other three bytes are ignored. Since all the requested bytes have not been accessed, the next word, which begins at 00B38 and contains bytes 00B38, 00B39, 00B3A, and 00B3B, is read from memory. Bytes 00B38, 00B39, and 00B3A fulfill the request; byte 00B3B is ignored.



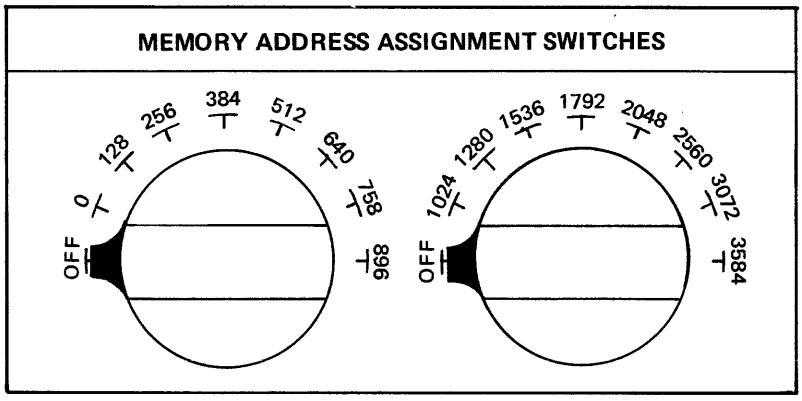
NOTE

> This request requires two memory cycles to access the four bytes. If the address of the first requested byte had been zero modulo four, only one memory cycle would have been needed, saving access time.

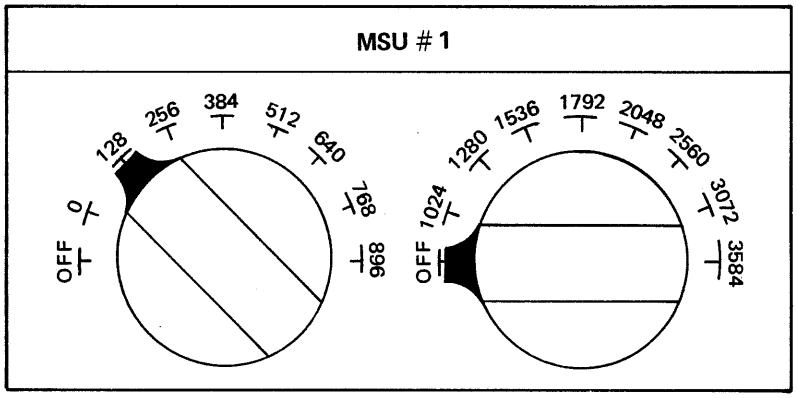
Memory Address Assignment Switches

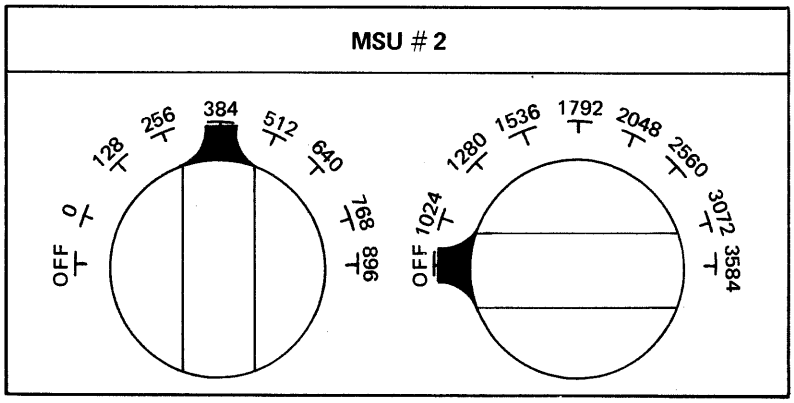
The storage capacity of an MSU is assigned a contiguous block of addresses within the total memory configuration. The addresses are assigned manually by setting the Memory Address Assignment Switches on the MSU control panel. Two switches are necessary to assign an MSU within the 0 - 4096K range of addresses. One switch is used for assigning addresses in the lower 1024K range; the other switch is used for assigning addresses in the upper 1024K - 4096K range. Corresponding memory ready indicator lights turn ON, on the operator's console, to indicate the range of MSUs that are in the ready state.

The following illustration shows the Memory Address Assignment Switches, followed by an explanation of the switch settings.



For example, assume that a 256K MSU is to be assigned to operate with addresses starting at 128K. Another MSU is to continue with sequential addresses where this MSU stops. The upper address range switch is placed in the OFF position; the lower address range switch is placed in the 128K position (starting address). The lower address range switch of the second MSU is placed in the 384K position, while the upper address range switch is in the OFF position.

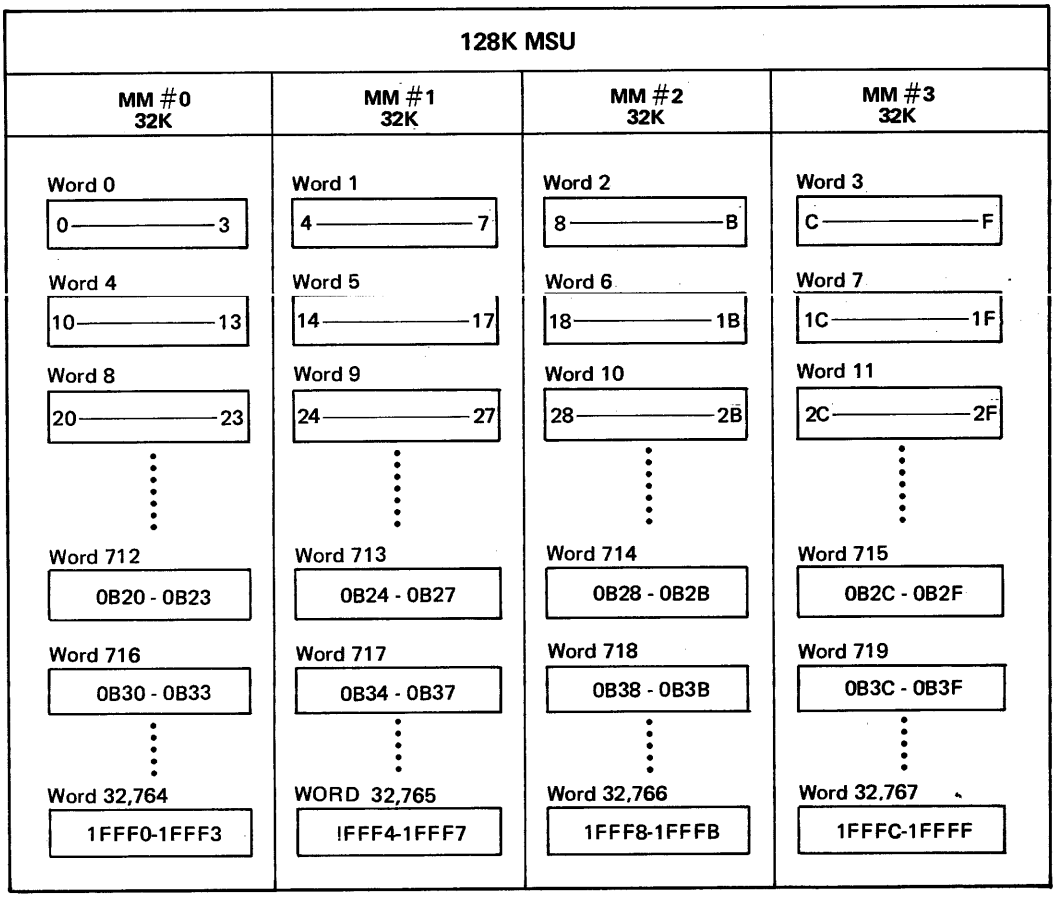




Memory Address Interleaving

Memory address interleaving is a concept where each successive word of data is stored in a different memory module. Data is interleaved among four memory modules. Every fourth word in a contiguous field is stored in the same module. Since each memory module is capable of cycling independently of the others, the accessing units (IOC, E unit, I unit) do not have to wait till the end of the memory cycle in one module before initiating a memory cycle in another module. Interleaving improves the efficiency of the processing units, and increases the memory throughput.

The following table shows the internal organization of the 128K MSU, with four 32K memory modules. As shown in the table, four contiguous words may be accessed, one in each module, before accessing the same module again. Word addresses are shown above the boxes in decimal notation, while byte addresses are shown within the boxes in hexadecimal notation.



The following illustration further exemplifies the advantages of memory address interleaving. The illustration shows all three processing units (IOC, E unit, I unit) accessing a different module simultaneously in the same MSU through their individual ports.

3-WAY SIMULTANEITY THROUGH MEMORY ADDRESS INTERLEAVING

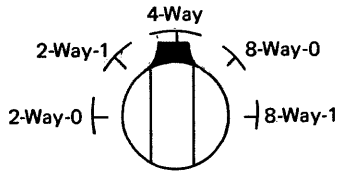
I Unit	MM #1 Word 1	MM #2 Word 2	MM #3 Word 3	MM #0 Word 4	MM #1 Word 5	MM #2 Word 6
E Unit	MM #2 Word 10	MM #3 Word 11	MM #0 Word 12	MM #1 Word 13	MM #2 Word 14	MM #3 Word 15
IOC	MM #3 Word 19	MM #0 Word 20	MM #1 Word 21	MM #2 Word 22	MM #3 Word 23	MM #0 Word 24

Mode Selection Switch

Normal operation in an MSU occurs in the 4-way interleaving mode, where each data word is stored in sequence in a different memory module, with every fourth word stored in the same module. In addition to the normal 4-way interleaving, two other modes of interleaving are available: 2-way interleaving and 8-way interleaving.

The mode of interleaving is selected by setting the Mode Selection Switch in the desired position. The Mode Selection Switch, located on the MSU control panel, has 5 positions, as shown in the illustration below.

MODE SELECTION SWITCH



In 2-way-0 mode, the MSU functions with the first two memory modules interleaved in a 2-way mode and the second two memory modules functionally removed from the system. In 2-way-1 mode, the MSU functions with the second two memory modules interleaved in a 2-way mode and the first two memory modules functionally removed from the system.

In the case of 2-way-0 mode, the words 0, 1, 2, 3, etc. are stored in modules 1-2, 1-2, and so on. In the case of 2-way-1 mode, the words are stored in modules 3-4, 3-4, and so on. The Mode Select Switch functionally removes either the first or the second pair of memory modules from the MSU. Half of a 256K or a 512K MSU is thus lost to the system; in case of a 384K MSU, 256K is lost to the system in either 2-way mode (0 or 1). A 128K MSU cannot be operated in the 2-way mode.

In the 4-way interleaving mode, which is the normal mode of operation for an MSU, data words are stored sequentially in alternating modules: modules 1, 2, 3, 4, then module 1 again, and so on in repetition to the full capacity of the MSU. In the 4-way mode of interleaving, as many as three processing units (IOC, E unit, I unit) can access the MSU simultaneously and cycle different memory modules, making this the most advantageous method of interleaving.

Operation in the 8-way interleaving modes is the least used of the five available modes of operation. 8-way interleaving is used when there are more than four accessing units to the MSU, as might be the case in a multiprocessing system. Although not used commonly, 8-way interleaving is possible in a single NCR Century 300 processing system. At least 2 MSUs are required for 8-way interleaving. Both MSUs have their Address Assignment Switches set to the same beginning address, and both MSUs must be of the same configuration (128K, 256K, or 512K). One MSU Mode Select Switch is put in the 8-way-0 position, while the other is put in the 8-way-1 position. In this mode, words 0, 1, 2, and 3 are stored in memory modules 1, 2, 3, and 4 of the first MSU, while words 4, 5, 6, and 7 are stored in memory modules 1, 2, 3, and 4 of the second MSU.

If during the operation of the system, it becomes necessary to change the mode of operation of an MSU, the entire memory must be reinitiated, because changing the Mode Select Switch settings may also affect the total memory available to the system and, therefore, the settings of the beginning addresses by the Address Assignment Switches in other MSUs. If a pair of MSUs is used in the 8-way mode, the range of addresses of the two MSUs is the sum of their individual ranges, and should be considered as such when assigning addresses to other MSUs in the system.

MEMORY TIMING

Memory cycle time is the time duration that is required from the start signal, that initiates a read or a write operation, till the end of the cycle when the memory module generates a memory ready signal, indicating that it is ready to initiate another cycle. Although the cycle time duration is a fixed value, within normal tolerances, determined during the design of the unit, the time to store or to retrieve data varies with respect to the processor. During a write operation, for example, the processing unit transmits and the memory unit accepts data early in the memory cycle. The data is stored in the data register of the memory unit until the actual setting of the cores is accomplished. The processor, however, has transmitted the data to the memory unit in a lot less time than is required to store it in core; therefore, the processor may initiate a new cycle in a different module before the module just accessed completes its function. This increases memory throughput and overall system efficiency.

Since the processing units are connected to the memory modules by interconnecting cables, the normal time that it takes to propagate a signal through wire and the delays associated with the transmitting and receiving logic-circuits are added to the total time it takes for the processing unit to access a memory module. There is a marked difference in time between the accessing times with reference to the processor and the accessing times with reference to the memory module itself.

The following table lists the various memory access times.

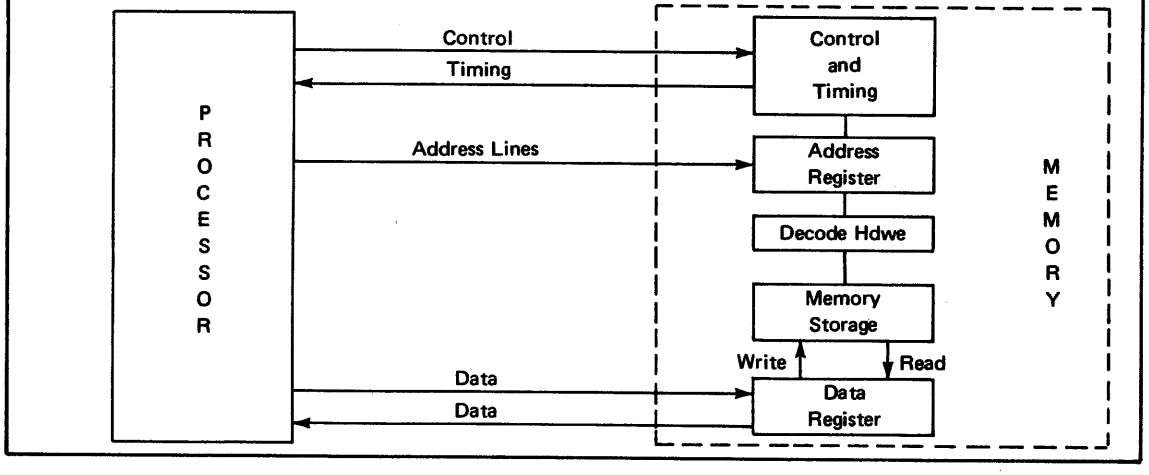
MEMORY CYCLE AND ACCESS TIMES		
Time Definition	**At Memory Module**	**At Processor**
Memory Cycle	680 NS	–
Write Access	100 NS	400 NS
Read Access	330 NS	730 NS

Another time, that by itself does not affect the memory cycle or access time, but does affect the overall memory throughput, is memory contention time. If more than one unit requires access to the same module, the one with the highest priority gains access first, which means that the other accessing unit(s) must wait until the completion of the present memory cycle, before being able to initiate the next one. This causes contention in memory accessing and a corresponding waiting period known as memory contention time. Memory contention time with one MSU in the system is approximately 110 nanoseconds. As the number of MSUs increases, the contention time decreases; if more than two MSUs are used in the system, the memory contention time is practically eliminated and may be ignored.

FUNCTIONAL OPERATION

The memory performs two basic functions: reading data and writing data. Each function requires one memory cycle. When the processor informs the memory that a read or a write operation is to be performed, hardware initiates a memory cycle. During the cycle, memory logic generates timing signals that govern the remainder of the operation. At the beginning of the cycle, the memory address register accepts an address from the processor, decodes it, and selects the proper location in the memory storage unit. During a read operation, the contents of the selected word are transferred to the data register where memory logic assembles the data into bytes and transmits them to the processor. During a write operation, the processor transmits the data to be stored in memory to the memory data register. Memory logic disassembles the data bytes and writes the information by bits into the specified locations.

MEMORY/PROCESSOR COMMUNICATION



Read Operation

A read operation is performed during one 680 nanosecond memory cycle. As the cycle progresses, the memory address register accepts the data address from the processor. This address specifies the memory location of the word that contains the requested byte(s). The data-bits in the selected word are sensed and stored in a memory data register. The contents of the data register are then transferred over data lines to the requesting unit (IOC E unit, I unit).

Write Operation

A write operation is also performed during a single memory cycle. As the cycle progresses, address selection is completed and the data to be written is transferred to the memory data register. Since only the selected byte positions in the memory data register can be altered, any remaining bytes in this register remain unchanged. During the next portion of the cycle, the altered word image in the memory data register is written into the original memory location.

Error Detection

To detect failures while reading data from memory storage, an additional bit (bit 9) is added to the eight data bits as the byte is stored in memory. This is the parity bit, generated by the parity generator logic in the processing unit, prior to the data transmission to memory. The bit is set ON (true) if the number of true data bits in the byte is even; the parity bit is set OFF (false) if the number of true data bits in the byte is odd. This assures that all bytes stored in memory have an odd number of true bits (called odd-parity). When data is read from memory, logic in the accessing unit checks the data bytes for an odd number of bits, which is indicative of a satisfactory read access. If any byte is found to contain an even number of bits, the Memory Error (ME) indicator is set ON and the processor enters an ME trapping routine. (For a detailed explanation of the ME trapping routine, see "Between-Commands Testing," in the ARITHMETIC-LOGIC PROCESSOR chapter, in this publication.)

The word format that appears in the MSU interface for storage in the memory module is shown below.

Byte 0	Byte 1	Byte 2	Byte 3
$p_0 b_{32}$--b_{25}	$p_1 b_{24}$--b_{17}	$p_2 b_{16}$--b_9	$p_3 b_8$--b_1

where p_0 through p_3 are the parity bits, and b_{32}--b_1 are the data bits.

The parity bits are not accessible to the program; their only function is to protect the integrity of the data stored in memory.

Since memory access is a word at a time, a full word is read and the parity bits checked for that word, even if the program calls for a partial word of data. During a write access, a parity bit is generated only for the bytes that are transmitted from the processing unit to the MSU for storage. The bytes that retain their original contents are restored to memory with their original parity bits.

OPTIONAL TIME OF DAY CLOCK (TOD)

An optional Time-of-Day Clock (TOD), which may be contained in the Memory Logic Panel (MLP) of any MSU, is normally contained in the control memory (0 - 128K) portion of the system. The TOD is an optional device that is required by the operating system for time-stamping messages, entries to the error log and other timed functions.

The TOD is enabled by a switch on the MSU control panel. A TOD available indicator light, also located on the MSU control panel, is lit when the switch is turned ON. The TOD is a freerunning, live 32-bit binary counter, incremented at 25 microsecond intervals, with an accuracy of ± .01%.

The TOD is accessed by initiating a memory access to address 264. When the TOD clock word (264-267) is addressed in memory, the TOD register is accessed rather than the memory module, and the contents of the register is made available to the processor. If a read operation is requested, the full word of the TOD clock register is transmitted to the ALP; a write operation causes the register to be reset to zero.

Since the TOD is a free-running register, incremented at 25 microsecond intervals, the actual time-of-day, during entry and display, is arrived at by software decoding the register output and converting it into hours and minutes.

ARITHMETIC LOGIC PROCESSOR (ALP)

INTRODUCTION

The Arithmetic Logic Processor (ALP) is composed of two functionally independent units: the instruction setup unit (I unit) and the execution unit (E unit). Each is an asynchronous unit which operates independently of and simultaneously with the other.

The I unit reads commands (program instructions) from memory, interprets these, and stores the associated information (partial operand address, addressing modes, data field lengths, etc.) in storage registers. Using the information specified in the command, the I unit computes the absolute memory addresses for each operand.

When command setup is completed, the I and the E units link in a mutually synchronized transfer flow, where the I unit transfers the information contained in the command, which it just completed setting up, to the E unit for execution.

The E unit performs the actual arithmetic (or other) calculation specified by the command. The actual steps involved in executing a given command are too numerous and variable to explain in this publication; for a detailed description of each command and its execution, refer to "NCR Century 251/300 Hardware Commands," under this tab.

INDEX REGISTERS

In the NCR Century 300, as well as all other models in this series, the operand addresses contained in the command are 2 bytes (16 binary bits) long. The maximum memory address that may be accessed by the operand address in the command, therefore, is 65,535 (binary 1111 1111 1111 1111 equals decimal 65,535).

With memory sizes exceeding 64K, the portions above 64K are addressed by modifying the addresses in the command. This is done by adding the address contained in the command, now referred to as partial address, to the contents of a register, referred to as an index register, which is large enough to access any location in memory.

All NCR Century series processors utilize 63 index registers, IR 1 through IR 63, which are contained in the main memory. Each index register consists of the three least significant bytes (24 bits) of a 4-byte word. The registers are in consecutive memory locations from 4 through 255.

The following illustration shows the index registers and their addresses in the main memory.

INDEX REGISTER LOCATIONS		
IR No.	IR Word Location	3-Byte IR Location
1	00004-07	00005-07
2	00008-11	00009-11
3	00012-15	00013-15
•	•	•
•	•	•
•	•	•
61	00244-247	00245-247
62	00248-251	00249-251
63	00252-255	00253-255

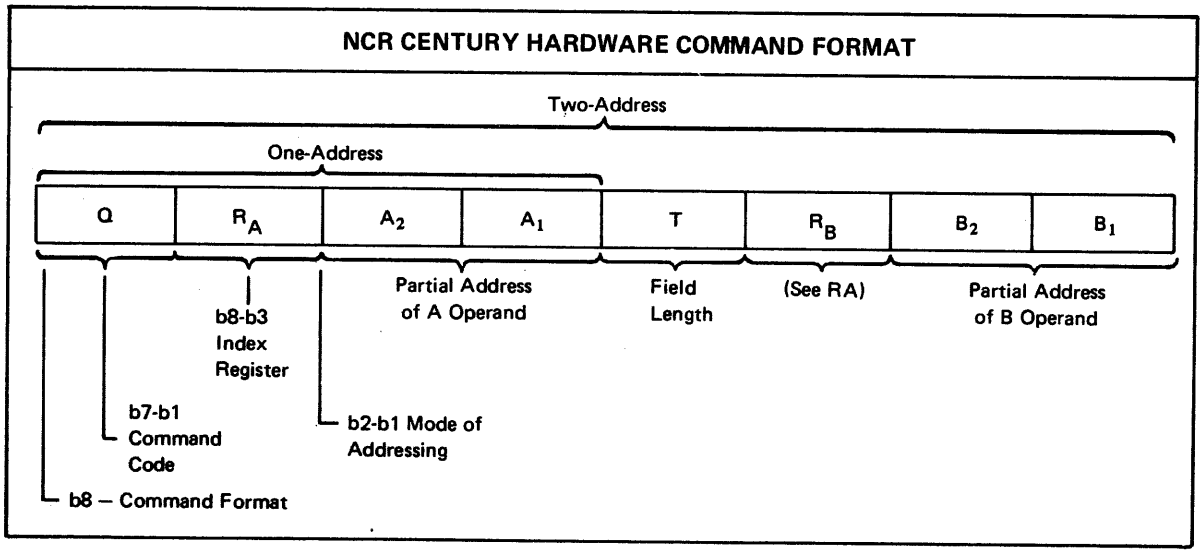
All index registers are accessible to the programmer and may be used as common memory storage areas. However, some of the index registers have been assigned for use with the operating system, so care must be taken not to destroy their contents. (See "Memory Registers" in this chapter.)

INSTRUCTION FORMAT AND INDEXING

The operating instructions are stored in memory as absolute (machine language) commands in 1- or 2-address formats, which occupy either 4 or 8 bytes of memory storage area. (1- or 2-address commands are also referred to as single- or double-stage commands.) Most commands require two addresses: an A operand address and a B operand address. (An add command, for example, requires the addresses of the two operands to be added.) The 1- and 2-address formats are functionally equivalent since the 1-address format uses the B operand address from the preceding command. In general, the results of an arithmetic operation replace the contents of the B operand address.

The address of the leftmost character (Command Code) of each command must be evenly divisible by 4 (0 mod 4). An attempt to execute a command that violates this rule results in a program error (PE) interruption.

The following illustration shows the format and contents of a two-address NCR Century command. The illustration is followed by an explanation and description of the functions of each byte within the command.



Command Code -- Q

The Q portion of the command specifies the command code and the command format. The binary value of b7 - b1 designates the command to be executed (add, subtract, etc.). The most significant bit (b8) indicates the command format:

- b8 = 0 The command has a 2-address format.
- b8 = 1 The command has a 1-address format; the address of the B operand and the length character (T), if required, are retained from the preceding command.

Index Register -- RA

The second byte of the command code contains the RA character. Bits 8 through 3 of the RA character specify an index register number from 0 through 63. When bits 8 through 3 specify an index register other than 0, the contents of the specified index register and the A2A1 portion of the command are added together to form the effective address. When bits 8 through 3 equal 0, the A2A1 portion of the command becomes the effective address.

The binary value of the b2 - b1 portion of the RA character specifies the mode of addressing:

- b2 - b1 = 0 Mode 0: Direct, non-incremental indexing
- b2 - b1 = 1 Mode 1: Indirect addressing
- b2 - b1 = 2 Mode 2: Indirect addressing
- b2 - b1 = 3 Mode 3: Direct, incremental indexing

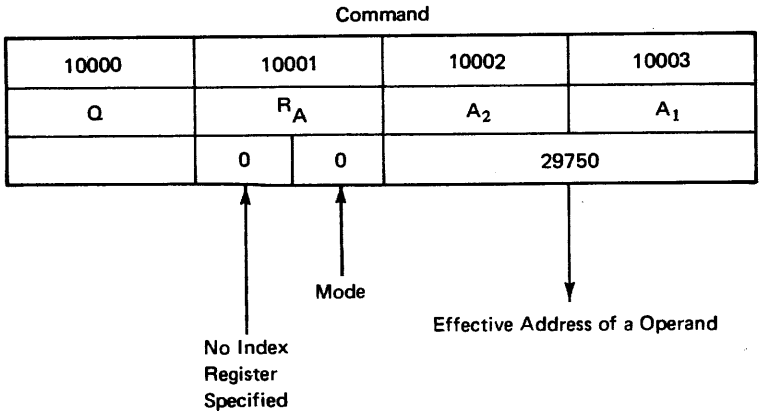
- Mode 0 Addressing

  If b8 - b3 = 0, no index register is specified, and the A2A1 characters contain the effective address.

  If b8 - b3 ≠ 0, the A2A1 characters are added to the contents of the specified index register to form the effective address; the contents of the specified index register remain unchanged.

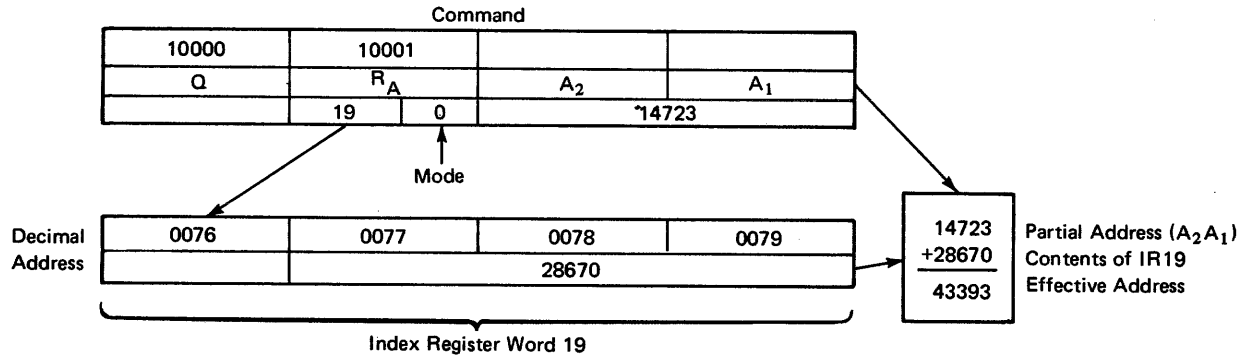
  EXAMPLE 1:

  Mode 0, no indexing (addresses are shown in decimal notation for simplification).



EXAMPLE 2:

Mode 0, Indexing



- Mode 1 Addressing

If b8 - b3 = 0, no index register is specified; the A2A1 characters form an effective indirect address.

If b8 - b3 ≠ 0, the A2A1 characters are added to the contents of the specified index register to form an effective indirect address; the contents of this index register remain unchanged.

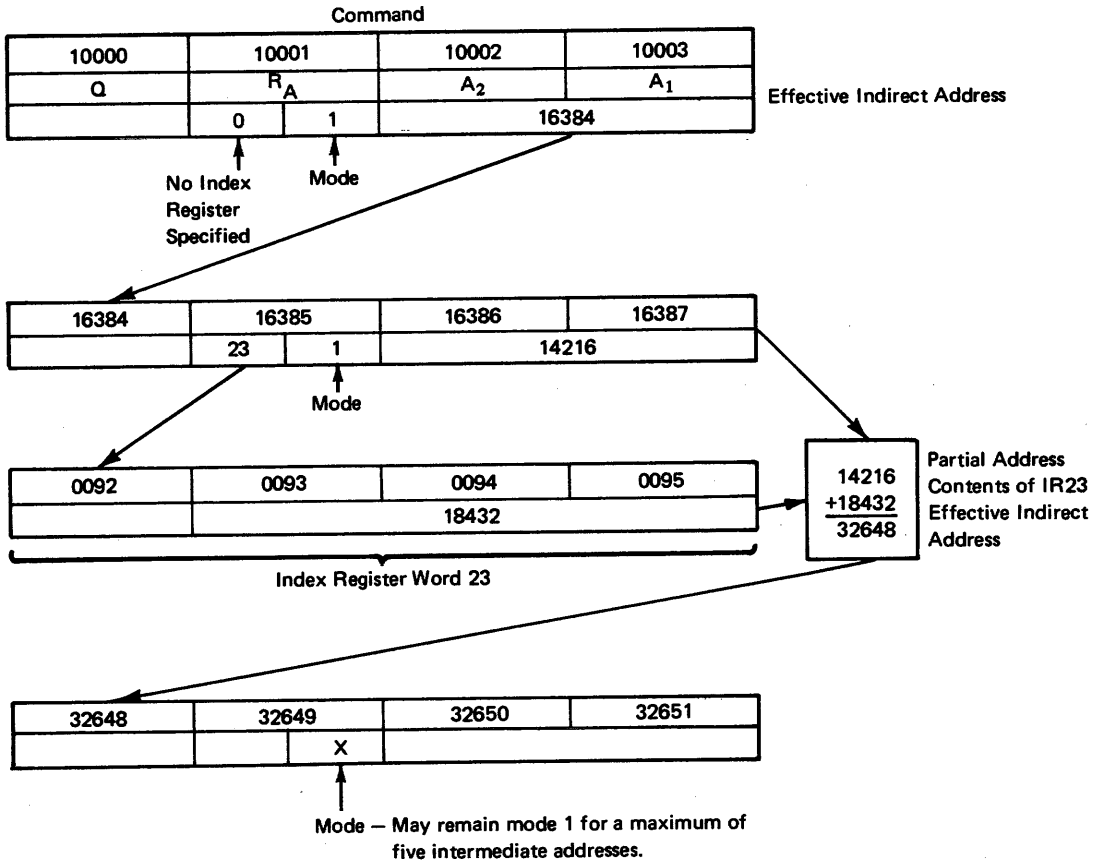
The contents of the 4-character address field specified by the intermediate effective address are read out of memory. The three least significant bytes of this 4-character field are now processed as the RA, A2, and A1 portion of the command. The mode of this 3-character address field determines whether the field contains the address of the A operand (mode 0) or whether the field contains another indirect address (mode 1). Mode 1 addressing can be repeated a maximum of five times; that is, five intermediate effective addresses can be used without a mode change. A PE occurs on the sixth repeat if no mode change is initiated.

The mode 1 addressing flow requires that the intermediate fields referenced must be at 0 mod 4 locations, otherwise a PE results.

A change to mode 0, 2, or 3 may be initiated at any of the intermediate fields referenced. Whichever mode is specified, the rule governing that particular mode is followed until the addressing flow is complete.

EXAMPLE:

Mode 1, no Indexing and Indexing



- Mode 2 Addressing

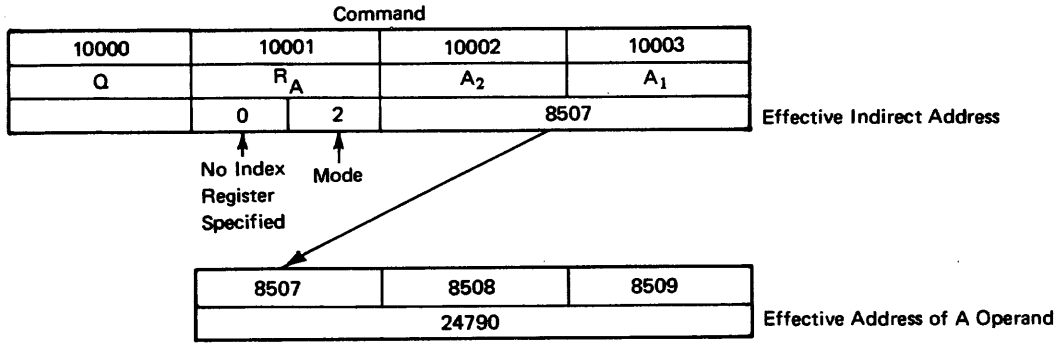
  If b8 - b3 = 0, no index register is specified; the A2A1 characters contain the effective indirect address.

  If b8 - b3 ≠ 0, the A2A1 characters are added to the contents of the specified index register to form an effective indirect address; the contents of the specified index register remain unchanged.

  The effective indirect address, which may be located anywhere in memory, specifies a 3-character field whose contents function as the effective address for that operand.

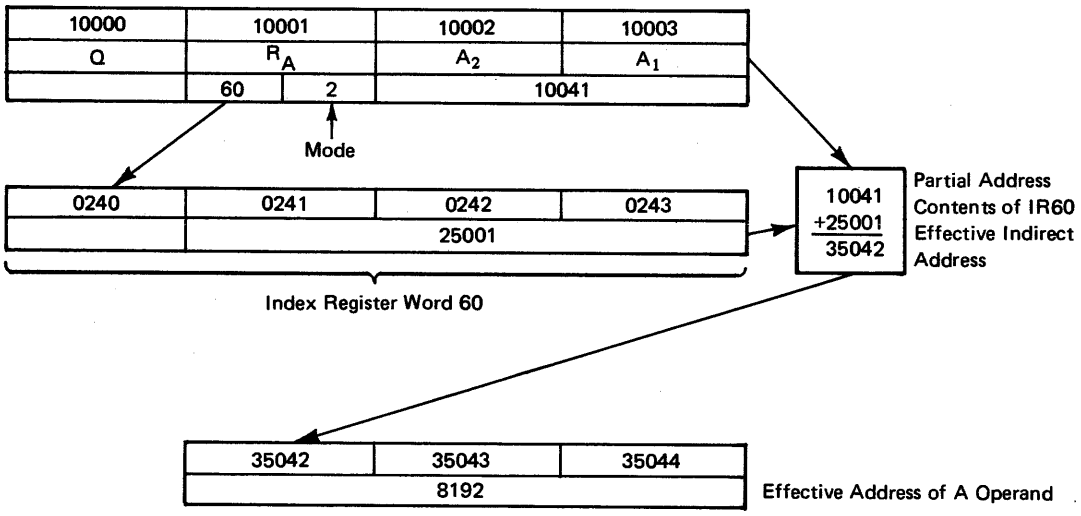
  EXAMPLE 1:

  Mode 2, no Indexing



EXAMPLE 2:

Mode 2, Indexing



- Mode 3 Addressing

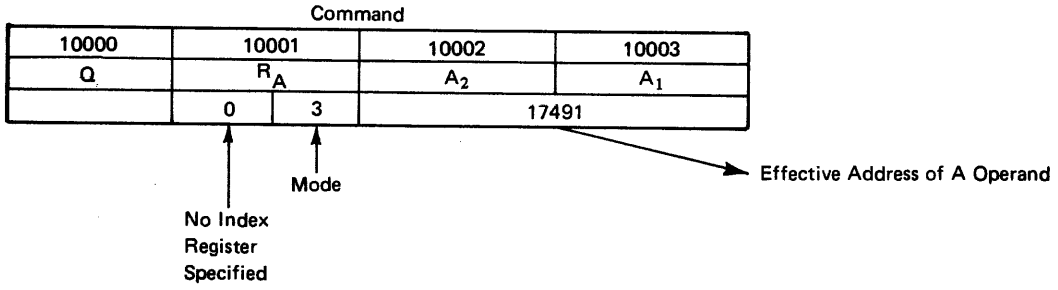
If b8 - b3 = 0, no incremental indexing is performed; the A2A1 characters contain the effective address.

If b8 - b3 ≠ 0, the A2A1 characters are added to the contents of the specified index register to form the effective address. The sum is then stored in the designated index register.

When command setup terminates, the address in the index register is equal to the effective A operand address. This technique is useful, for example, in stepping through tables.

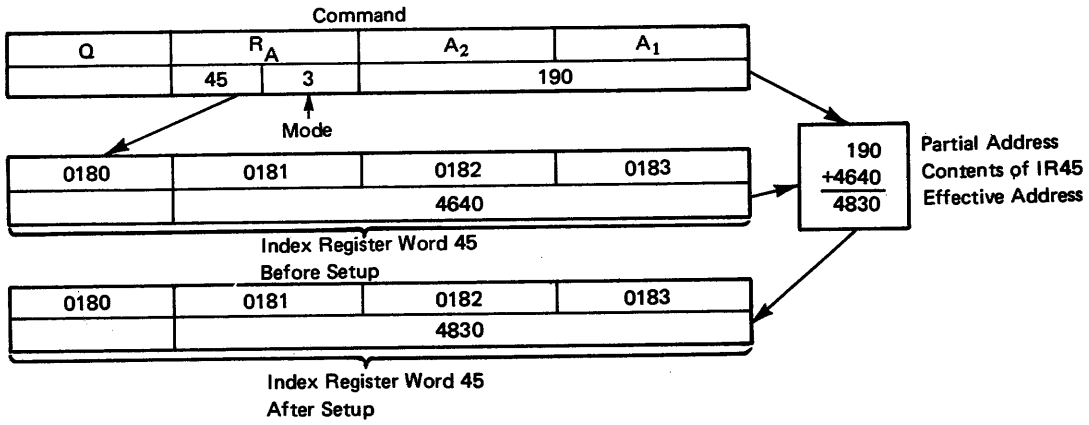
EXAMPLE 1:

Mode 3, no Indexing



EXAMPLE 2:

Mode 3, Indexing



For added flexibility in addressing, all NCR Century series processors provide the ability for decremental indexing as well as incremental indexing. Decremental indexing, for example, may be used to search through a table in descending order.

During command setup, the contents of the specified index register are added to the contents of the command operand address (A2A1 or B2B1) to form the effective address. The two addresses are considered as unsigned binary fields. Decrementing is accomplished by adding the quantity (65,536 - n) to the contents of the index register; n is the value of the desired reduction (decrementation). Since the index registers in the NCR Century 300 are 24-bit registers and the command operand address is a 16-bit field, the value of bit 16 is added to bit positions 17 through 22 of the index register. No carry is propagated beyond the 22nd bit position during addition, and the contents of bit positions 23 and 24 of the index register remain unchanged. In the following illustration, the address in the index register is decremented by 10, by adding the partial address 65,526 (65,536 - 10).

DECREMENTAL INDEXING

Bit Position	24 23 22 21 20 19 18 17 16 15 14 13 12 11 9 8 7 6 5 4 3 2 1
Partial Address 65,526 (65,536-10)	① ① ① ① ① ① 1 1 1 1 1 1 1 1 1 1 1 0 1 1 0
Contents of IR 131,072	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	* C C C C C
Effective Address 131,062	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 0

C = Carry, generated as a result of adding the partial address to the contents of the specified index register.
* = No carry generated from the 22nd bit position.

When indexing is performed, the partial address contained in the A2A1 or B2B1 portion of the command may be considered to be a "displacement" from

the base address contained in the index register. Since the value of the 16th bit of the partial address is added to bits 17 through 22 of the index register during decremental indexing, only bits 1 through 15 are included in the displacement value configuration. As a result, the maximum displacement values are -32,768 (decremental) and +32,767 (incremental). As shown in the following illustration, a positive displacement value is equal to the partial address; a negative displacement value is subtracted from 65,536 to arrive at the partial address. If the maximum displacement values are exceeded, the resulting effective address is not directly related to the sum of the partial address and the base address.

EFFECTIVE ADDRESS CALCULATION BY DISPLACEMENT

Displacement Value	Partial Address	IR Contents	Effective Address
30,000	30,000	30,000	60,000
-00,005	65,531	30,000	29,995
32,767	32,767	32,768	65,535
-16,384	49,152	32,768	16,384
* 65,500	65,500	30,000	29,964
** -65,500	00,036	70,000	70,036

* When the positive displacement limit is exceeded, the resulting effective address does not reflect the desired incrementation of 30,000 by 65,500 (29,964 rather than 95,500).

** When the negative displacement limit is exceeded, the resulting effective address does not reflect the desired decrementation of 70,000 by 65,500 (70,036 rather than 4,500).

A2A1 Characters

This is a 2-character binary field representing the partial address of the A operand. If the RA character designates neither indexing nor indirect addressing, the A2A1 characters form the effective address of the A operand.

Length -- T

The binary value of the T portion of the command specifies the field length, in bytes, of the A and B operands. T is an eight bit character ranging in value from 0 to 255 with 0 usually considered equal to 256. The use of T and the length specified by T are discussed in detail for each command in the publication "NCR Century 251/300 Hardware Commands," under this tab.

Index Register -- RB

The RB character is identical to RA, except that it pertains to the B operand rather than the A operand.

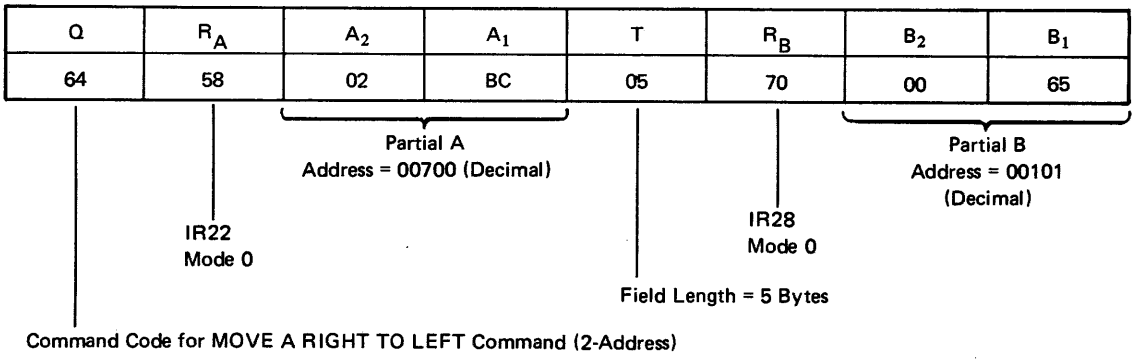
B2B1 Characters

The B2B1 characters are identical to A2A1, except that they pertain to the B operand rather than the A operand.

NOTE

Any mode of addressing, with or without indexing, may be used to derive the effective A operand address and the effective B operand address, independently of each other.

EXAMPLE:



During a command setup, the I unit computes the effective addresses of the A and B operands.

Assume that the two index registers contain the following information:

(IR22) = 0AF0 (02800)
(IR28) = 0898 (02200)

0AF0 + 02BC = 0DAC (03500) Effective A address
0898 + 0065 = 08FD (02301) Effective B address

Operand contents before command execution:

A =

03500	03501	03502	03503	03504
00110100	00110001	00110010	00110110	00111001

B =

02301	02302	02303	02304	02305
00110001	00110010	00110110	00111001	00110000

Following execution of the MOVE A RIGHT TO LEFT command, the initial contents of A have replaced the initial contents of B. The contents of A are unchanged:

A =

03500	03501	03502	03503	03504
00110100	00110001	00110010	00110110	00111001

B =

02301	02302	02303	02304	02305
00110100	00110001	00110010	00110110	00111001

Since the command specifies no incremental indexing, the contents of IR22, and IR28 remain the same. (If the command had specified incremental indexing for both operands, then the contents of IR22 would be ODAC, and the contents of IR28 would be 08FD at the termination of the command.)

Implied T and B Operation

All commands that terminate in a normal manner leave predictable T and B values available for use by subsequent commands. Except for the RESTORE command, the T value available following command setup is not changed during command execution.

The B value depends upon the specific command executed; it too, however, is predictable according to the conventions described in the "NCR Century 251/300 Hardware Commands," under this tab. Any command may be coded in a 1-address format once a preceding 2-address command has established the B and T characters. The setup of the 1-address command does not disturb these values, and they are used as if they were part of the current command. This characteristic permits strings of 1-address commands to be "chained" to a 2-address command as illustrated in the following example.

EXAMPLE:

Implied T and B Operation

A MOVE, ADD, and COMPARE command are in consecutive memory locations.

Q	R_A	A_2	A_1	T	R_B	B_2	B_1
64	00	03	E8	02	00	07	D0

MOVE A RIGHT TO LEFT -- Each character in the field specified by the A address is moved into the field specified by a B address, one character at a time, starting with the rightmost character.

Q	R_A	A_2	A_1
C0	00	08	B8

ADD SIGNED -- The A field and the B field are added decimally; the result replaces the B field. (The B and T values have been established by the preceding MOVE command.)

Q	R_A	A_2	A_1
C5	00	0F	A0

COMPARE SIGNED -- The A field is compared to the B field. (The B and T values have been established by the MOVE command.)

PROCESSOR OPERATION

Besides the use of fast-switching, quick-responding integrated circuit components and other advanced developments in computer technology, the NCR Century 300 achieves high internal processing speeds by implementing the following operational methods in the ALP.

- Asynchronous Operation -- Both processing units (E and I) of the ALP perform their operations asynchronously; that is, each unit performs its operations timed by an internal clock, without waiting for an external clocked synchronizing signal.

- Simultaneity -- The processing units of the ALP function simultaneously: the I unit sets up a program instruction from memory, while the E unit executes the previous instruction. Because of this overlap of time, functions that theoretically would require a certain amount of time, if done sequentially, are now done in half that time, concurrently.

- Word Processing -- A word (4 bytes) of data is processed at a time. This includes memory read and write operations, addition, subtraction, comparison, all other command functions, and data transfer between memory, IOC, E unit, and I unit.

Additional speed is achieved by using numerous live (hardware) registers, with their time-saving, zero-delay access feature, throughout the ALP for quicker address, data, and other information manipulation. Live registers perform their functions without the delays encountered in accessing memory for the desired information.

Due to the volume of information that must be saved for the operating system software (index registers, tables, flags, etc.) and hardware (trap addresses, error status words, etc.), it is impractical to store this much information in live registers. For this reason, a portion of memory is reserved for privileged information, necessary for the proper operation of software and hardware.

Live Registers

Hardware live registers permit the processor to access their contents with zero time-delay. The use of live registers to limit memory accesses only for data and program instructions facilitates the asynchronous operation of the NCR Century 300 processor. Live registers required for command execution, for example, are loaded by the I unit during the command setup phase and transferred to the E unit for use during the execution phase. The following table contains a list of live registers, their location, and their contents.

PROCESSOR LIVE REGISTERS				
Term	Name	I Unit	E Unit	Contents
CR	Sequence Control Register	X	X	Address of the Next Command to be Executed
LA	A Address Register	X	X	Effective A Operand Address
LB	B Address Register	X	X	Effective B Operand Address
LB*	Original B Address		X	Original Effective B Address
T*	Length Register	X		Original T of the Command
T TA TS	Tally Registers		X	T Character Counted Up or Down During Command Executions
D	Tally Modifier Register		X	Values Used to Modify the Tally Register
LC	Miscellaneous Register		X	Miscellaneous Register Used by the E Unit
L	Memory Address Register	X	X	Memory Address to be Accessed
A	Address Modifier Register		X	Value Used to Modify the Memory Address Register
Q	Command Code Register	X	X	Command Code Byte
IRA	Index Reg. Number	X		Index Register Number Specified By the RA Byte of the Command
IRB	Index Reg. Number	X		Index Register Number Specified By the RB Byte of the Command
CRA	Miscellaneous Control Register	X		Address Specified by the Sequence Control Register During the Setup of the A Portion of the Command
CRB	Miscellaneous Control Register	X		Same as CRA, for the B Portion of the Command
BAR	Base Address Register	X	X	Beginning Address of a Program Segment in Memory (Used in Multiprogramming)

LB* Original value of B operand; used in command chaining.
T* Original value of T; used in command chaining.

PROCESSOR LIVE REGISTERS (CONT'D.)				
Term	Name	I Unit	E Unit	Contents
LAR	Limit Address Register	X	X	Maximum Length of a Program Segment in Memory (Used in Multiprogramming)
MN	Monitor Register	X		Address of a Memory Location. A Trap Condition Occurs when this Location is Written Into
F	F Register	X	X	An Input to the Adder
GA	GA Register	X	X	An Input to the Adder
GB	GB Register		X	Data Register (Shift Logic)
JA	Data Register	X	X	Memory Input/Output Register
JB	Data Register		X	Data Storage Register
SH	Shifter	X	X	Shift Register for Data Manipulation

Memory Registers

Memory registers, in reserved areas of the internal memory, contain data such as program status words, the error status word, control words and commands. The 63 standard index register reside in this area. The processor requires a memory cycle to obtain one word of information from or transfer one word of information into these registers. The following illustration is a memory map of the reserved areas of memory and an explanation of their contents.

RESERVED MEMORY AREAS

Contents	Index Register	Decimal Address	Hex Address	Contents Character	Explanation
	IR#0	00000 To 00003	0000 To 0003		Not Used
Reserved Index Registers	IR#1 To IR#4	00004 To 00019	0004 To 0013		Reserved Registers Used by Software
Error Status Word (ESW) Program status that is stored when PE or ICC trapping flow is entered	IR#5	00020	0014	Q	Command Code
		00021	0015	A	Effective A Address
		00022	0016		
		00023	0017		
	IR#6	00024	0018	T	Field Length
		00025	0019	B	Effective B Address
		00026	001A		
		00027	001B		
		00028	001C	Flags	b1 = "Less" Flag b2 = "Equal" Flag b3 = "Greater" Flag b4 = Trace Permit Flag b5 = Repeat Indicator b6 = Overflow Flag b7 = Not Used b8 = Supervisor Flag
	IR#7	00029	001D	CR	Control Register
		00030	001E		
		00031	001F		
Error Status Word (ESW) Program status that is stored when ME trapping flow is entered		00020	0014	Q	Command Code
		00021	0015	Special Flags	b8 = 0 ME Occurred During E Unit Access b8 = 1 ME Occurred During I Unit Access b7 = 0 Single ME During I Unit Access if b8 = 1 b7 = 1 Multiple ME during I unit access if b8 = 1
	IR#5	00021 (b1-b6)	0015 (b1-b6)		Absolute Address Where ME was Detected
		00022	0016		
		00023	0017		
	IR#6	00024	0018		Contents of the Absolute Address Stored in IR#5
		00025	0019		
		00026	001A		
		00027	001B		
		00028	001C	Flags	b1 = "Less" Flag b2 = "Equal" Flag b3 = "Greater" Flag b4 = Trace Permit Flag b5 = Repeat Indicator b6 = Overflow Flag b7 = Not Used b8 = Supervisor Flag
	IR#7	00029	001D	CR	Control Register
		00030	001E		
		00031	001F		

RESERVED MEMORY AREAS (CONT'D.)

Contents	Index Register	Decimal Address	Hex Address	Contents Character	Explanation
		00032	0020	RC	Repeat Counter
Link Register	IR#8	00033 00034 00035	0021 0022 0023	L	Return Link is Stored When Jump Command is Executed
		00036	0024	EC	Error Code Storage b1 = PE b2 = Illegal Command Code (Illegal Command) b3 = Not Used b4 = Illegal Command Code (Privileged Command Violation) b5 = Not Used b6 = F. P. Attempt to Divide by Zero b7 = F. P. Characteristic Underflow b8 = F. P. Characteristic Overflow
Next Address Index Register	IR#9	00037 00038 00039	0025 0026 0027	NAIR	Next Address Stored by Decode and Scan Commands
Program Status Word (PSW)		00040	0028	Q	Command Code
	IR#10	00041 00042 00043	0029 002A 002B	A	Effective A Address
		00044	002C	T	Field Length
Program Status Stored by Program Interrupt	IR#11	00045 00046 00047	002D 002E 002F	B	Effective B Address
		00048	0030	Flags	See Error Status Word
	IR#12	00049 00050 00051	0031 0032 0033	CR	Control Register
		00052	0034	Q	Command Code
Program Status Word (PSW)	IR#13	00053 00054 00055	0035 0036 0037	A	Effective A Address
		00056	0038	T	Field Length
Program Status Stored by Trace Interrupt	IR#14	00057 00058 00059	0039 003A 003B	B	Effective B Address
		00060	003C	Flags	See Error Status Word
	IR#15	00061 00062 00063	003D 003E 003F	CR	Control Register

RESERVED MEMORY AREAS (CONT'D.)

Contents	Index Register	Decimal Address	Hex Address	Contents Character	Explanation
		00064	0040	CC	Count Counter (Count Command)
Index Registers #16 through #63 Used as Nondedicated Word Registers	IR#16	00065 00066 00067	0041 0042 0043		
	IR#63	00252 00253 00254 00255	00FC 00FD 00FE 00FF		
ME Control Area		00256 00257 00258 00259	0100 0101 0102 0103		The Least Significant 22 Bits Contain Address to Which Control is Transferred When ME Occurs
PE Control Area		00260 00261 00262 00263	0104 0105 0106 0107		The Least Significant 22 Bits Contain Address to Which Control is Transferred When PE Occurs
Time of Day Clock Word		00264 00265 00266 00267	0108 0109 010A 010B		Special Time of Day Clock Word
		00268 To 00271	010C To 010F		Not Used
Interrupt Control Area		00272	0110	II & IP	b8 = Pseudo II b1 = Pseudo IP
		00273 00274 00275	0111 0112 0113	IC	The Least Significant 22 Bits Contain Address to Which Control is Transferred When a PI Occurs
Trace Control Area		00276 00277 00278 00279	0114 0115 0116 0117	TC	The Least Significant 22 Bits Contain Address to Which Control is Transferred When Tracing Trap Or Address Monitor Trap Occurs
Table Address		00280 00281 00282 00283	0118 0119 011A 011B		Table Address Used by Table Compare Command
		00284 To 00319	011C To 013F		Not Used
Memory Accumulator		00320 To 00335	0140 To 014F		Memory Accumulator Used By Multiply, Divide, and F. P. Commands
Interval Timer CW		00336 To 00343	0150 To 0157		Special Control Word Used with the Interval Timer
		00344 To 00383	0158 To 017F		Not Used

RESERVED MEMORY AREAS (CONT'D.)					
Contents	Index Register	Decimal Address	Hex Address	Contents Character	Explanation
Termination Queue Pointer		00384 To 00447	0180 To 01BF		Termination Queue Pointer Words
		00448 To 01023	01C0 To 03FF		Not Used
Control Word Area		01024 To 01031	0400 To 0407		Control Word 0
		03064 To 03071	0BF8 To 0BFF		Control Word 255
		03072 To 05119	0CC0 To 13FF		Optional for Additional 256 Control Words

Flags and Indicators

Various flags are used throughout the NCR Century 300 to denote the results of setting up the operands of a command, indexing mode considerations, user/supervisor state, the results of a compare command, and other conditions. Indicators, which are similar to flags, denote repeat conditions, command code trap conditions, error conditions, etc. Some flags and indicators have console indicator lights which show the state of the flag and/or indicator. The following table gives the name, type, and definition of the flags and indicators used in the NCR Century 300 processing system.

PROCESSOR FLAGS AND INDICATORS			
Term	Name	Console Indicator	Function
RI	Repeat Indicator	Yes	Indicates a repeat of a command.
IP	Interrupt Permit	Yes	Set on by the program to permit interrupt of the main program to handle peripheral termination.
II	Interrupt Indicator	Yes	Indicates that a peripheral termination occurred. If IP was not set on previous to the termination, the interrupt is not serviced.
TP	Trace Permit	Yes	Indicates that each command executed is being monitored.
ME	Memory Error	Yes	Indicates that an error was encountered while reading data from memory.
PE	Program Error	Yes	Indicates a programmer error condition.

PROCESSOR FLAGS AND INDICATORS (CONT'D.)

Term	Name	Console Indicator	Function
EI	Error Indicator	Yes	Indicates an unrecoverable error condition. If EI and either ME or PE is on the processor halts.
ICC	Illegal Command Code Indicator	No	Indicates an unrecognized command code ; a trap routine is entered.
	Test IOC Test ALP	Yes Yes	Indicates that the OPERAT/MAINT. switch is in the MAINTENANCE position.
	Halt	Yes	Indicates that processor is in HALT state.
	Wait	Yes	Indicates that processor is executing the WAIT command.
	Monitor	Yes	Indicates that MONITOR switch is on.
	Load Error	Yes	Indicates that manual load terminated with an S3 status other than OPERATION COMPLETE.
	CRT-Keyboard	Yes	Indicates that the keyboard is logically connected to the CRT.
	CRT-Input	Yes	Indicates selection of CRT for input.
	CRT-Local	Yes	Indicates selection of CRT for local input by operator.
	I/O Writer Keyboard	Yes	Indicates that the keyboard is Logically connected to the I/O Writer.
	I/O Writer Input	Yes	Indicates selection of the I/O Writer for input to memory.
	I/O Writer Output	Yes	Indicates selection of the I/O Writer for output from memory.
	Hex	Yes	Indicates data interpretation as two hexadecimal characters per byte.
	Alpha	Yes	Indicates data interpretation as one alphanumeric character per byte.
L	Less Than	Yes	Indicates a "less than" condition during a compare or scan command.
E	Equal To	Yes	Indicates an "equal to" condition during a compare, scan, or decode-to-delimiter command.
G	Greater Than	Yes	Indicates a "greater than" condition during a compare, or a decode-to-delimiter command.

PROCESSOR FLAGS AND INDICATORS (CONT'D.)

Term	Name	Console Indicator	Function
OF	Overflow	Yes	Indicates a condition where the adder function resulted in an output bit configuration greater than the output register (JA) of the adder.
S	Supervisor	Yes	Indicates the state of the processor.
A	Flag A	No	Used in conjunction with the S flag. If flag A is on it indicates BAR/LAR processing for the A value.
B	Flag B	No	Used in conjunction with the S flag. If flag B is on it indicates BAR/LAR processing for the B value.
	Console Ready	Yes	Indicates a manual console function.
EH	Hardware Error	Yes	Indicates detection of an error in the IOC or console.
	Load	Yes	Indicates a manual load in progress.
	Display	Yes	Indicates selection of the CRT or I/O Writer in the display mode.
	Enter	Yes	Indicates selection of the CRT or I/O Writer in the enter mode.
	Touchplate	Yes	Indicates selection of the touchplate switches by system software.

I UNIT

The I unit is an independent asynchronous unit which sets up a command for execution by the E unit. In addition to command setup, the I unit performs limited command execution (LOAD MONITOR REGISTER).

Command Setup

During the setup phase, the I unit reads the first four bytes (1 word) of the command specified by the sequence control register and stores these in their respective registers. Depending on the logical decisions made according to the contents of the Q, RA, A2, and A1 characters, the I unit performs modification and indexing of the A operand address, determines whether the command is in 1- or 2-address format, checks the validity of the A operand address, and performs other related setup functions. After setting up the first half

of the command (command code, A operand address), the I unit proceeds to set up the second half (operand length, B operand address), if required. If the T value and the B operand address are implied from a previous command, the setup phase for the T value and B operand address is omitted.

Unit-to-Unit Transfer and Interpretation

Upon completion of the command setup, the I unit and the E unit enter the transfer flow. In this flow, the information from the command stored in the live registers of the I unit is transferred to the live register of the E unit. The E unit interprets the Q portion of the command to determine which command execution flow to enter.

During the transfer flow, the ALP performs extensive tests for error and certain transfer-of-control conditions, which are explained under "Between-Commands Testing," below.

E UNIT

The E unit is an independent asynchronous unit which executes the command previously set up by the I unit.

Command Execution

The exact functions of the E unit depend on the interpretation of the Q character. The actual steps involved in executing a given command are too numerous and variable to explain in this publication; for a detailed description of each command and its execution, refer to "NCR Century 251/300 Hardware Commands," under this tab.

BETWEEN-COMMANDS TESTING (BCT)

Introduction

Depending on the results of the tests performed in between-commands testing, the processor either alters its program flow, halts, or continues the program flow.

The ALP tests certain error conditions, transfer-of-control indicators, and the halt indicators, in the following sequence, according to their priority:

1. Error Indicator (EI) and one of the following:
    - Memory Error (ME)
    - Programming Error (PE)
    - Illegal Command Code (ICC)
2. Memory Error (ME)
3. Programming Error (PE)
4. Illegal Command Code (ICC)
5. Repeat Indicator (RI)
6. Trace Permit (TP)
7. Interrupt Indicator (II) and Interrupt Permit (IP)
8. Halt

The Error Indicator (EI), Memory Error (ME), Programming Error (PE), or Illegal Command Code (ICC) are set as a result of a command malfunction. Command malfunctions are those detected during command setup, execution, or between-commands testing, rather than those detected during the I/O flow. The Repeat Indicator (RI), Trace Permit (TP), and Interrupt Permit (IP) are set under program control as a result of executing the corresponding command. The Interrupt Indicator (II) is set by the IOC as a result of a peripheral terminating an I/O operation, The Halt indicator is set when the processor enters the Halt state or when the operator sets the HALT switch on the console.

Functional Operation

If, during between-commands testing, any of the conditions tested are met (one or more indicators are turned ON), the processor either halts or enters a trapping flow to alter its normal program flow. If none of the conditions are met (the indicators are OFF), the processor continues its normal program flow.

A trap is an automatic transfer of control to a specified memory location as a result of specific conditions detected by hardware. The memory location to which control transfers is the starting address of a software routine designed to handle the condition that caused the trap.

The current status of the program at the time of trapping is stored in reserved index registers as the status word. The status word enables the processor to reenter the program flow later at the point where the trap condition occurred. There are two types of status words:

- Program Status Word (PSW) -- The current status of the program is stored in locations 040-051, if a Program Interrupt is initiated, or in locations 052-063, if a Trace Trap is taken.
- Error Status Word (ESW) - The current status of the program is stored in locations 020-031, if a command malfunction occurs (ME, PE, or ICC Trap). The ESW is stored in two formats, one for an ME and the other for a PE and ICC Trap, as shown in the RESERVED MEMORY AREAS table, under the heading "Memory Registers," in this chapter.

NOTE

> The Repeat condition, explained in detail later in this chapter, is the only exception to the functional operation just described.

Error Indicator (EI)

The error indicator (EI) is turned ON, under certain conditions, by a command malfunction. If another command malfunction occurs while the EI is ON, the malfunction cannot be processed (recovered from) and the processor enters an error halt state.

As the trapping flow is entered, the indicator that caused the entry is turned OFF. An ME or a PE trapping flow turns ON the error indicator (EI). An Illegal Command Code (ICC) does not turn ON the EI unless a PE is detected while in the trapping flow.

If a command malfunction occurs while in the trapping flow, the appropriate indicator is turned ON again. During between-commands testing in the transfer flow all indicators are tested. The EI being set indicates that the processor is in an error recovery routine. An ME, PE, or ICC being set indicates a command malfunction during the recovery routine. This constitutes a double error condition which causes the processor to enter a halt state.

In the halt state the I/O control becomes inactive. Peripherals terminate their activity in the same manner as they do when their request for service is not answered.

The EI is turned OFF by a JUMP command or by the System Reset Switch on the operator's console.

Memory Error (ME)

The detection of a memory error causes the ME Indicator to be set ON. Normally the erroneous character remains undisturbed; that is, it still has incorrect parity. However, the erroneous character is altered in the two instances listed below:

- The character containing the ME is one of the index register characters used when incremental indexing mode (mode 3) has been specified.
- The character containing the ME is one of those characters in the error status word.

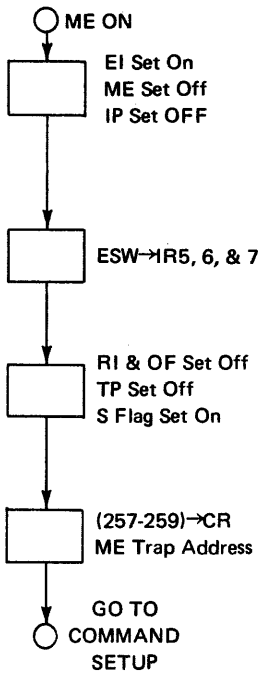
In both instances, the character containing the ME will be replaced by a different character with correct parity before the next command is accessed.

If during between-commands testing the error indicator (EI) is OFF, and the memory error indicator (ME) is ON, the processor enters the ME trapping flow. Upon entering this trapping flow, the EI is set ON, the ME is set OFF, and the IP is set OFF.

The significant state of the processor, the error status word (ESW), is stored in memory locations 020-031; IR 5, 6, and 7.

The repeat indicator (RI), the overflow flag (OF) and the trace permit (TP) are set OFF. The Supervisor (S) flag is set ON.

The control register (CR) is loaded with the contents of memory locations 257-259. These locations contain the address of the first command of the ME trap routine. Command set-up is then entered for this command.



Program Error (PE) and/or Illegal Command Code (ICC)

The detection of a programming error during command setup and execution causes the PE indicator to be set ON. The current operation is terminated and between-commands testing is begun.

An illegal command code, detected by the ALP, is a command code which is not included in the set of hardware commands, or which belongs to a privileged command (refer to "Privileged Commands," under MULTIPROGRAMMING FEATURE in this chapter. The detection of an illegal command code causes the illegal command code indicator (ICC) to be set ON, the current operation to be terminated, and between-commands testing to be started.

If the program error (PE) and/or the illegal command code (ICC) is ON during between-commands testing, the PE and the ICC trapping flow is entered. Depending upon the cause of the trap, one of the following error codes will be stored in memory location 036:

TRAPPING ERROR CODES

Cause of Trapping	Memory Location 036							
	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1
PE	0	0	0	0	0	0	0	1
ICC (not previleged)	0	0	0	0	0	0	1	0
PE and ICC (not privileged)	0	0	0	0	0	0	1	1
ICC (privileged)	0	0	0	0	1	0	0	0
PE and ICC (privileged)	0	0	0	0	1	0	0	1
Floating Point Attempt to Divide by Zero	0	0	1	0	0	0	0	1
Floating Point Characteristic Underflow	0	1	0	0	0	0	0	1
Floating Point Characteristic Overflow	1	0	0	0	0	0	0	1

Bits 3 and 5 are not used and are set to zero.

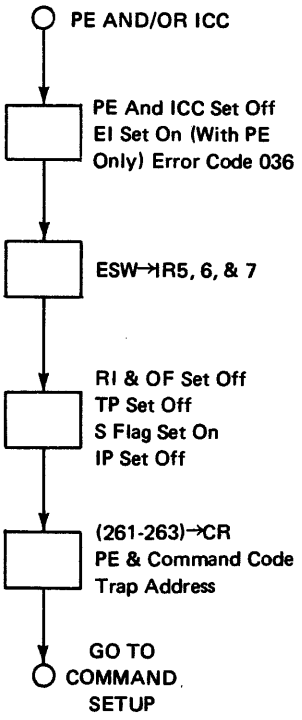
If the trap was caused by a PE, the PE indicator is set OFF, the error indicator (EI) is set ON, and the error code is stored in memory location 036.

If the trap was caused by an illegal command code, ICC is set OFF, EI is left undisturbed, and the error code is stored in memory location 036.

If the trap was caused by both an illegal command code and a PE, the ICC and PE are set OFF, EI is set ON, and the error code is stored in memory location 036.

The significant state of the processor, the error status word (ESW), is stored in memory locations 020-031; IR 5, 6, and 7. The repeat indicator (RI), overflow flag (OF), the trace permit (TP) indicator, and the interrupt permit (IP) are set OFF. The Supervisor (S) flag is set ON.

The control register (CR) is loaded from memory locations 261-263. These locations contain the PE and ICC trap address, which is the address of the first command of the PE and ICC trap routine. Command setup is then entered for this command.



Repeat Indicator (RI)

The repeat indicator (RI) is set ON during the REPEAT command if the number of times specified for execution of the next command in sequence (command to be repeated) is other than 0.

A repeat counter (RC), memory location 032, stores the number of times a command is to be repeated. This counter is decremented by 1 each time the repeated command is executed. When the repeat counter equals 0, repeating terminates.

A secondary repeat indicator (RII) is also set ON during the REPEAT command. It is used when one of the following commands is to be repeated:

BINARY COMPARE
COMPARE SIGNED
TEST BIT
TEST CHARACTER EQUAL
TEST CHARACTER UNEQUAL
SCAN
TABLE COMPARE

If the conditions as stated in one of these commands are satisfied before the repeat counter becomes equal to 0, the secondary repeat indicator is turned OFF, allowing the repeating to terminate.

If the repeat indicator is ON following the execution of any command except the REPEAT and RESTORE commands, the between-commands repeat flow is entered.

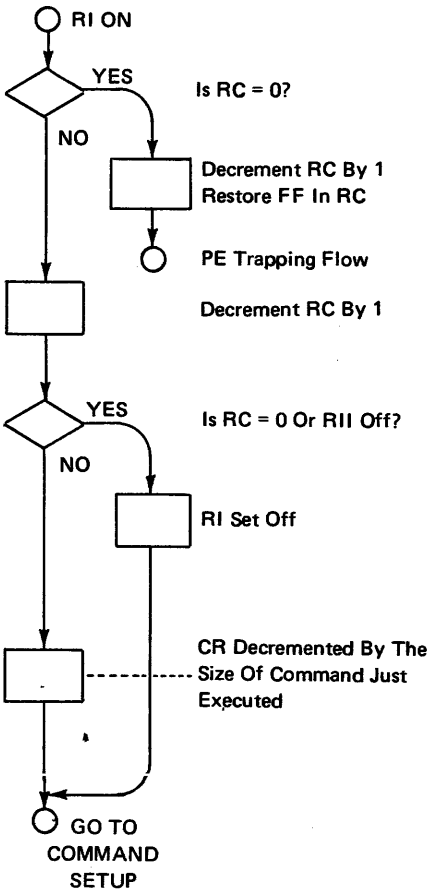
The repeat counter memory location, 032, is read out and tested for 0. If it is 0, a PE results; however, the repeat number in the RC is decremented by 1 and restored as FF (hex) in the RC before the processor enters the PE trapping flow.

If the repeat counter is other than 0, it is decremented by 1 and restored in memory.

The repeat counter is tested again for 0 and the secondary repeat indicator is tested.

If the test indicates that the repeat counter is 0 or that the secondary repeat indicator is OFF, the repeat indicator is set OFF and the operation terminates (the control register has been updated to address the next command). Command setup is then entered for this next command.

If the test indicates that the repeat counter is not 0 and the secondary repeat indicator is ON, the control register is decremented by the size of the command just executed, thereby causing the same command to be re-executed.



Trace Permit (TP)

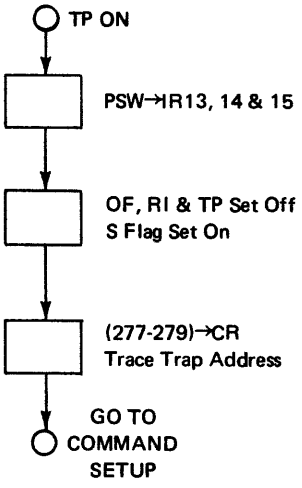
The trace permit flag is tested by the processor during between-commands testing, and, if it is ON, the trace interrupt flow is entered.

The trace feature provides the ability to monitor each command execution when the trace permit (TP) flag is ON. The feature includes three additional machine commands, two of which can be used for setting or resetting of the trace permit flag. The third command gives the trace feature the ability to specify a memory location that is monitored when the MONITOR switch is ON. Writing into this memory location causes trapping to occur by setting the trace permit flag ON. This memory location may also be specified from the console.

Upon entering the trace interrupt flow, the significant state of the processor, the program status word (PSW), is stored in memory locations 052-063; IR 13, 14, and 15.

The overflow flag (OF), repeat indicator (RI) and trace permit (TP) are set OFF. The Supervisor (S) is set ON.

The control register (CR) is loaded with the contents of memory locations 277-279, the address of the first command of the trace trap routine.



Command set is then entered for this command.

Pressing the LOAD switch on the console causes the trace permit (TP) to be turned OFF.

Interrupt Permit (IP) and Interrupt Indicator (II)

Between-commands testing can interrupt the normal flow of a program to enable the interrupt routine to process the termination of I/O operations.

Interrupt permit (IP) may be set ON or OFF by program control to indicate the state of the program's readiness to accept an interrupt. IP is also set OFF by the interrupt trapping flow (to prevent the interrupt flow from being interrupted by another termination) and by the console LOAD switch.

The interrupt indicator (II) is set ON to designate that the I/O control has detected a terminating status signal or a latent error condition. (For a detailed description of the latent error condition, see "S4 Status Character" in the I/O Control chapter of this publication.) The II remains ON until the processor enters the interrupt routine.

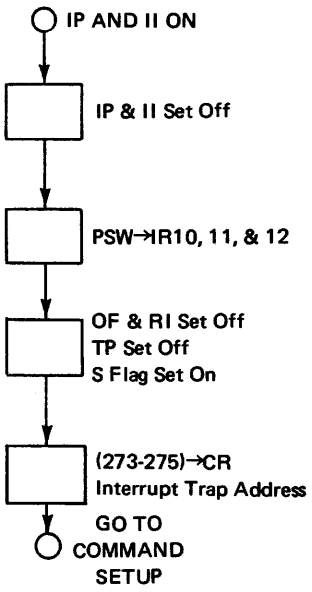
If, during between-commands testing, the interrupt permit and interrupt indicator are both ON, the processor enters the interrupt trapping flow.

Upon entering the trapping flow, IP nnd II are both set OFF.

The significant state of the processor, the program status word (PSW), is stored in memory location 040-051; IR 10, 11, and 12.

The overflow flag (OF), repeat indicator (RI), and trace permit (TP) are set OFF. The Supervisor (S) flag is set ON.

The control register is loaded with contents of memory locations 273-275, the address of the first command of the interrupt trap routine. Command setup is then entered for this command.



- Pseudo II and IP

  Software, in conjunction with the IP ON and the IP OFF commands, uses pseudo II's and pseudo IP's to service I/O terminations. The pseudo II and the pseudo IP are stored in bits 8 and 1, respectively, of relative memory location 272. Each user's partition in memory contains these pseudo indicators. The use of pseudo II and pseudo IP allows the user to determine whether or not he wants to interrupt his program to service an I/O termination.

Halt

If the HALT switch is ON and none of the aforementioned conditions (EI, ME, PE, etc.) exist, the processor enters the halt state at the completion of between-commands testing. (Upon exit from the halt state, the processor enters between-commands testing again.)

TRACE FEATURE

Tracing is a diagnostic aid that helps to analyze the execution of a program. The trace feature in the NCR Century 300 provides a means to monitor each command execution. Each step of a program may be monitored and interpreted by the trace trap routine, and information printed out about it.

When used with the monitor switch on the console, selective trace is available, where the contents of a specified memory location is monitored. If that location is written into, the processor enters the trace trapping routine to interpret and print out about the information in the specified memory location.

The trace feature includes the trace permit (TP) indicator and three hardware commands: STORE TRACE, LOAD TRACE, and LOAD MONITOR REGISTER.

Trace Execution

When the trace permit (TP) indicator is ON, the processor hardware performs the following functions during each BCT (Between-Commands Testing):

- The state of the processor is stored in the program status word (location 0052-0063).
- The overflow flag (OF), the repeat indicator (RI), and the trace permit (TP) indicator are turned OFF.
- The S-flag is turned ON.
- The control register (CR) is loaded with the starting address of the trace trap routine (0277-0279).

The hardware functions of BCT for trace are then complete and the processor enters the trace trap routine.

If a memory error (ME) occurs during the readout of memory locations 0277-0279, the ME indicator is turned ON, the control register remains undisturbed, and the ME trap routine is entered.

If locations 0277-0279 contain an illegal address (greater than memory size or not zero modulo four), the CR is loaded with the illegal address. The subsequent program error trap stores this illegal address in the Program Status Word (PSW) as the contents of the control register.

Initiating Trace

The trace feature is under program control. By using the LOAD TRACE and STORE TRACE commands, the program can turn the TP indicator ON or OFF. With the TP indicator ON, the trace trap routine is entered from BCT. With the TP indicator OFF, tracing is not initiated.

Initiating Selective Trace

When the trace feature is used with the Monitor Switch on the operator's console, the processor enters the trace trap routine only when a specified memory location is written into. The memory location address that is so monitored is stored in the Monitor Register, which may be loaded by program instruction (LOAD MONITOR REGISTER), or manually from the operator's console.

With the Monitor switch set ON, the TP indicator is turned ON when the memory location specified by the contents of the Monitor Register is written into. With the TP indicator ON, the processor enters the trace trap routine, as explained previously under "Trace Execution".

The two exceptions, when the TP indicator is not turned ON, are:

- The processor is in a hardware trapping flow.
- The monitored memory location is written into by the IOC during an I/O operation.

When the Monitor switch if OFF, the Monitor Register has no effect and tracing is not initiated.

FLOATING POINT FEATURE

General

The floating point hardware feature for the NCR Century 300 System automatically scales the numbers involved in a computation and maintains the precision of the result of the computation. The feature comprises 12 commands that provide for addition, subtraction, comparison, multiplication, multiplication-addition, and division.

A floating point number is expressed as a signed hexadecimal fraction multiplied by a power of 16:

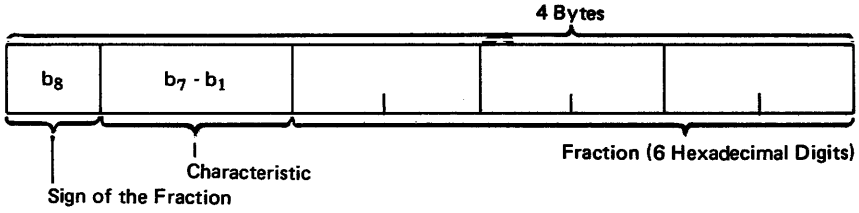
$$\pm .F \times 16^{n}$$

where "± .F" represents the signed fraction and "n" represents the exponent (power) to which the base, 16, is raised.

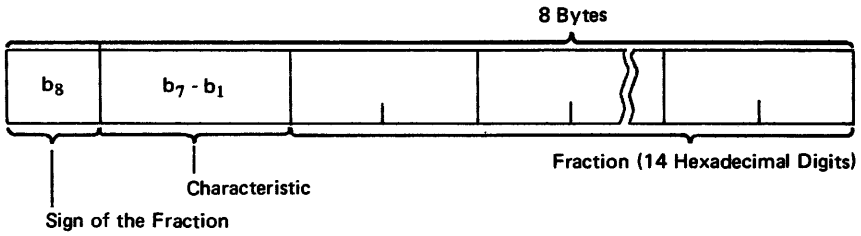
Floating Point Format

Floating point numbers occupy fixed-length formats as either 4- or 8-byte fields:

Single Precision



Double Precision



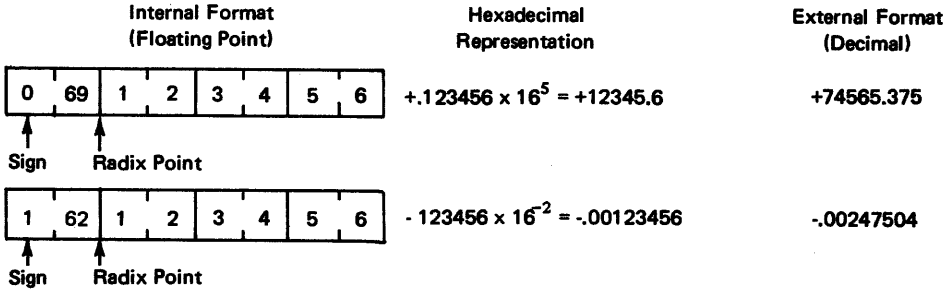
Sign of the Fraction

If b8 = 0, the sign is positive.
If b8 = 1, the sign is negative.

Characteristic

The characteristic is a 7-bit binary number that specifies the power by which the base, 16, is exponentiated. The exponent is expressed in "excess 64" notation. That is, a characteristic of 64 represents the zero power, 65 represents a power of one, and so on. Since the characteristic ranges from zero through 127, the exponent thus represented ranges from -64 through +63.

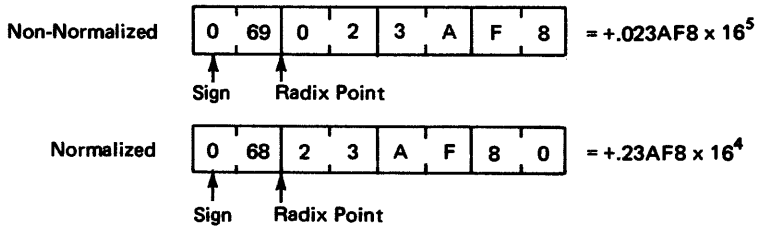
The amount by which the characteristic exceeds (or falls short of) binary 64 determines the number of positions the radix point is scaled to the right (left) of the leftmost hexadecimal digit of the fraction and, as a result, the number of positions the decimal point is moved to the right (left) of the leftmost digit when the number is converted to external format.



Fraction

The fraction consists of either six (single precision) or 14 (double precision) hexadecimal digits. The radix point is positioned between the characteristic and the leftmost digit of the fraction, and is scaled to the left or right by the value of the characteristic. The number is generally "normalized"; i.e., adjusted so that no leading zeros exist between the most significant digit and the radix point.

The decimal number 9134.5 is expressed in hexadecimal notation as 23AF.8. It is shown in both normalized and non-normalized floating point format below.



The maximum and minimum limits of the characteristic, together with the maximum and minimum limits of a single precision hexadecimal function, result in an absolute range of magnitude for floating point numbers, which is 00 100000 (normalized) through 127 FFFFFF. In double precision, the limits are 00 10000000000000 through 127 FFFFFFFFFFFFFF. Thus a floating point number is capable of expressing any decimal number within the range of (approximately) $\pm 5.4 \times 10^{-79}$ through $\pm 7.2 \times 10^{75}$.

Floating Point Fractional Number Representation

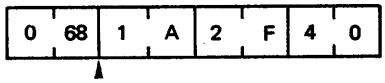
Fractional floating point numbers are hexadecimal expressions which, when removed from internal floating point format (radix point scaled to left or right according to the value of the characteristic), have one or more non-zero digits remaining to the right of the radix point.

Two types of fractional numbers may be represented in floating point notation -- mixed numbers and pure fractions.

- Mixed Numbers

  Mixed number representations result in hexadecimal expressions that, when removed from floating point format, have one or more digits on both sides of the radix point. This type of hexadecimal expression represents a decimal number that consists of a whole number and a decimal fraction, as in the following single precision floating point representation.

  Floating point format----------



  Which represents the hexadecimal expression----------

  Which, when removed from floating point format, equals----------

  Which is equal to the decimal value----------

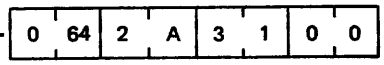
  NOTE

  The actual method of conversion from hexadecimal to a decimal value is explained on the following pages.

- Pure Fraction Numbers

  Pure fraction representations result in hexadecimal expressions that, when removed from floating point format, have one or more digits to the right (only) of the radix point. This type of hexadecimal expression represents a decimal fraction, as shown in the following single precision floating point representation.

  Floating point format----------



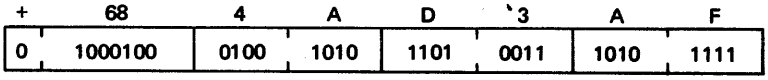
  Which represents the hexadecimal expression----------

  Which, when removed from floating point format, equals----------

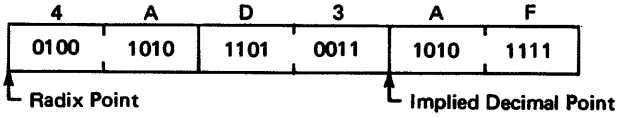
  Which is equal to the decimal value----------

Floating Point Number Conversion

A floating point representation of a decimal number is converted to its decimal equivalent by the following method: First, the characteristic is examined; each unit of difference between the characteristic and binary 64 indicates one hexadecimal digit between the decimal point and the established position of the radix point (preceding the leftmost digit of the floating point fraction). For example, the floating point number that appears in memory as:

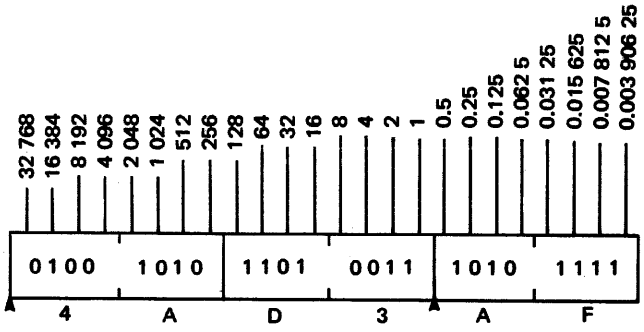


indicates, by its characteristic of 68, that the decimal point is to be positioned four hexadecimal digits to the right of the radix point, resulting in the hexadecimal number shown below.



(A characteristic less than 64 indicates that the decimal point is located an appropriate number of digits to the left of the radix point. Since no digits exist to the left of the radix point's established position, these nonexistent digits are presumed to have a value of zero.)

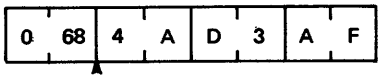
Next, each bit of the resulting hexadecimal number is given a value that is equal to a power of two, corresponding to the bit's position in relation to the adjusted radix (decimal) point. For example, the bit immediately preceding the decimal point is valued at 2^0, the next bit to the left is given a value of 2^1, and so on to the most significant bit. To the right of the decimal point, the first bit is valued at 2^{-1}, the next at 2^{-2}, and so on to the least significant bit of the fraction. The following is an illustration of the bit values for the number shown above.



Each bit is examined and, if it is "true," its value is added to an accumulating total. This total is the decimal equivalent of the floating point representation. This step in the conversion process of the above number is illustrated below.

16384.	
2048.	
512.	
128.	
64.	
16.	
2.	
1.	"True" bit values to left of decimal point
0.5	"True" bit values to right of decimal point
0.125	
0.03125	
0.015625	
0.0078125	
0.00390625	
19155.68359375	Sum of all "true" bit values = decimal equivalent

Finally, the algebraic sign expressed by the first bit of the floating point number is applied to its decimal equivalent. Thus, the floating point number



is the equivalent of the decimal number +19155.68359375.

Conventions

All floating point commands (except FLOATING POINT COMPARE SINGLE and FLOATING POINT COMPARE DOUBLE) produce normalized results. Any floating point number may therefore be normalized by adding it to floating point zero.

Since only hexadecimal digits can be normalized, the three leftmost bits of a normalized fraction may be zero.

Although single precision floating point words have a 6-digit fraction, intermediate results in addition, subtraction, and division may be expressed with 7-digit fractions. The seventh (rightmost) digit is a guard digit that increases the precision of the final result. This guard digit is not stored after termination of the operation; a guard digit is not used in double precision operations.

The results of add and subtract commands replace the contents of the original B operand. No other floating point commands disturb either the A or B operand, nor, except for those commands that store into a memory accumulator, is any memory character other than the referenced floating point words ever affected.

A positive number with a zero characteristic and a zero fraction is a true zero. A true zero may result because of the particular magnitude of the operands. A result is forced to be true zero when an exponent underflow occurs or when a result fraction is zero.

If a result has a zero fraction, overflow of the characteristic will not cause the PE trap that would otherwise occur.

If a divisor has a zero fraction, division is inhibited and a PE trap occurs. Otherwise, zero fractions and zero characteristics are treated as normal numbers in all arithmetic operations.

A zero fraction will not result from any operation except as part of a true zero; if a number having a zero fraction and a non-zero characteristic is introduced, an incorrect operation may result.

MULTIPROGRAMMING FEATURE

Multiprogramming is a technique of programming where two or more programs share the time and resources of a computer.

Generally, programs have to wait for the completion of an I/O operation, since the external devices are much slower than the central processor. Because programs are generally I/O bound, it is advantageous to have more than one program resident in memory in such a way that while some programs wait for the completion of their I/O requests, another may use the resources of the central processor. Hence, the technique of multiprogramming -- sharing the time and resources of a computer by two or more programs resident in memory.

Multiprogramming is a standard hardware feature of the NCR Century 300. By reducing the ALP idle time, multiprogramming significantly increases the productivity of the system. Because the ALP resources are not devoted to a single program, the NCR Century 300 system can provide economical realtime online services to many users.

To switch efficiently from one program to another, to allocate memory space, and to protect the memory area allocated to one program from interference by other programs, the NCR Century 300 uses a combination hardware-software multiprogramming method. The discussion of multiprogramming which follows deals primarily with hardware features; software is mentioned only where required for clarity and understanding.

Program Switching

When a processor switches from one program to another, it must save the status of the interrupted program, including the index registers and private data. Switching programs in this manner causes a large software overhead.

The NCR Century 300 accomplishes program switching by use of both software and multiple BAR/LAR hardware registers. A BAR (Base Address Register) contains the beginning (lowest) address of a program segment in memory, and a LAR (Limiting Address Register) contains the length of this segment, thereby establishing the upper limit of the segment. When giving control to a new program, rather than save and restore the current program's index registers and private data, the Executive program changes the contents of the BAR/LAR registers to refer to the memory area where the new program is located. This results in large savings in software overhead when switching programs.

Memory Allocation

The multiprogramming operating software determines memory space requirements, peripheral requirements, and other pertinent requirements of the program, according to the parameters entered during system initialization. Software then allocates the memory and the peripherals as efficiently as possible. During the process of loading the various programs into memory, the operating software logs their beginning and ending addresses in a BAR/LAR reference table.

When switching to a particular program, the system software accesses the BAR/LAR reference table and loads the values associated with that program into the BAR/LAR registers.

Since memory space is allocated dynamically and the addresses in a compiled program are relative to the contents of the BAR/LAR, the programmer may write his programs with the starting address relative to zero.

Memory Protection

Each program is protected against accidental or intentional interference by other programs. Protection is provided by the BAR/LAR registers and by the use of two flags: the Write Prohibit Flag and the Segment Unavailable Flag. Each program is assigned a BAR/LAR value for its lower and upper limit boundary, respectively. Only the system Executive can change the contents of the BAR/LARs, which ensures that each program's memory area is not violated.

Each BAR/LAR contains a Write Prohibit Flag and a Segment Unavailable Flag. The Write Prohibit Flag prohibits writing into that memory segment. The Segment Unavailable Flag has a dual function:

- It serves as a read and write prohibit flag to prevent any segment in memory from being accessed by an unauthorized program.
- It is used to mark the BAR/LARs that are not used by a program.

Supervisor/User State

For increased efficiency in executing multiple programs, the NCR Century 300 utilizes two modes of operation -- user and supervisor.

The processor is always in either the user or the supervisor state. The state of the supervisor flag (S-flag) determines in which state the processor is. If the S-flag is ON, the processor is in the supervisor state. If the S-flag is OFF, the processor is in the user state. In the user state, the processor executes the customer programs normally. In the supervisor state, the processor handles special conditions that cannot be completed in the user state. Whenever the processor encounters conditions that require special handling, it turns ON the S-flag and enters the supervisor state. The following flows cause the S-flag to be turned ON:

- Program Interrupt
- ME Trapping
- PE Trapping
- Trace Trapping
- ICC Trapping
- Console Loading

When the processor resumes normal processing, the S-flag is turned OFF by a RESTORE command, and the processor enters the user state.

Privileged Commands

Certain commands, called Privileged Commands, may be executed only in the supervisor state, because they require special handling under software control. An attempt to execute a privileged command in the user state causes the processor to take the ICC Trap. The following are privileged commands:

- INOUT (Initiate I/O)
- INOUT (Load Priority Register)
- WAIT
- SWITCHES INPUT
- LOAD BAR
- LOAD MONITOR REGISTER

Status Word

All trapping flows store the state of the S-flag in bit 8 of the ninth character of the Status Word. The S-flag is stored in the state it was in prior to entering the flow, ignoring any change that may occur in the flow. The contents of the ninth character of the status word are:

- b8 S-flag
- b7 Always OFF
- b6 Overflow Flag
- b5 Repeat Indicator
- b4 Trace Flag
- b3 Greater Flag
- b2 Equal Flag
- b1 Less Flag

The remaining characters of the status word are explained earlier in this chapter and are shown in the memory map.

Memory Segmentation

The NCR Century 300 contains five BAR and five LAR registers, designated as BAR/LAR X, 0, 1, 2, and 3. Each BAR is a 14-bit register. LAR X is a 4-bit register, while the remaining LAR registers contain 11 bits. The BAR/LAR registers contain addresses in increments of 256, as if they had 8 zero bits appended to the right. Although it is possible to partition memory into five segments by use of the BAR/LAR registers, their implementation is software-dependent.

The following illustration shows the possible minimum and maximum memory segment sizes obtainable through the use of BAR/LAR registers.

MEMORY SEGMENTATION BY BAR/LAR

Segment Number	Minimum Size	Maximum Size
X	256 bytes	3,584 bytes
0	256 bytes	520,704 bytes
1	256 bytes	524,288 bytes
2	256 bytes	524,288 bytes
3	256 bytes	524,288 bytes

BAR/LAR X is dedicated to the index register segment of individual programs. Since the index registers and private data are located within the virtual addresses of 000000 - 003583 of all NCR Century programs, this BAR/LAR is selected for addressing whenever the virtual effective address falls in this range. The virtual effective address is the operand address after indexing but before BAR addition.

BAR/LAR 0 is used for addressing user code. For compatibility purposes it is selected for addressing whenever the virtual effective address falls in the range of 003584 - 524,287.

The remaining BAR/LAR registers are assigned by software as required.

BAR/LAR Usage

- Relative Addressing

  Each program contains the A and B addresses and the addresses of the control registers used by the program in "relative" form, rather than in absolute form. If required, addition of the BAR register contents to these addresses occurs prior to a memory access. The A, B, or CR values stored in the Program and the Error Status Words are unaffected by the BAR register contents. (The Error Status Words, Program Status Words, and Error Code Characters are stored in a system software area; their addresses are not subject to BAR/LAR manipulation.)

- BAR Selection

  In the user state (S-flag OFF) all memory accesses from the processor are subject to BAR addition. In the supervisor state (S-flag ON) memory accesses are subject to BAR addition under certain conditions, described later in this section.

  When a BAR is used, its contents form a base address to which a relative address is added to form an absolute address. For each BAR, the corresponding LAR specifies the upper limit address. The bit configuration of the relative effective address specifies a BAR/LAR register as shown in the following illustration.

BAR/LAR SELECTION

Bit Configuration								BAR/LAR Selected
b_{24}	b_{23}	b_{22}	b_{21}	b_{20}	$b_{19\text{-}13}$	$b_{12\text{-}9}$	$b_{8\text{-}1}$	
0	0	0	0	0	0	*	X	X
0	0	0	0	0	**	X	X	0
0	0	0	0	1	X	X	X	1
0	0	0	1	0	X	X	X	2
0	0	0	1	1	X	X	X	3

X = any value
* = $b_{12\text{-}9} \leq 1101$
** = $b_{19\text{-}13} > 0000000$, or $b_{12\text{-}10} = 111$

Bits 24, 23, and 22 of the virtual effective address must be zero or a PE occurs.

Once a specific BAR is selected for an operand during the execution of a command, that BAR is used for all memory accesses made for that operand. This ensures that all virtual effective memory addresses for each operand fall within a single segment of memory. If not, a PE occurs.

- LAR Check

When BAR X is selected, the contents of LAR X are compared to the contents of bits 12-9 of the virtual effective address. If the contents of LAR X are equal to zero or are greater than the contents of bits 12-9, the BAR value is added to the virtual effective address and the memory access is permitted. If the virtual effective address is equal or greater, a PE occurs.

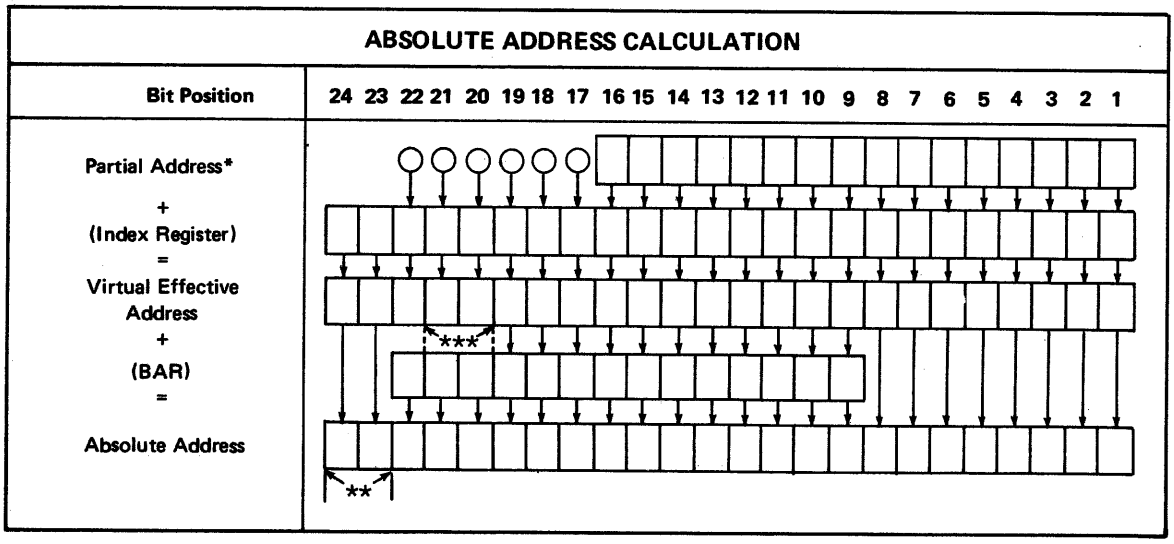
Similarly, when BAR 0, 1, 2, or 3 is selected, the contents of LAR 0, 1, 2, or 3, respectively, are compared to the contents of the address bits 19-9 of the virtual effective address. If the contents of the LAR are equal to zero or greater than the contents of bits 19-9, the memory access is permitted. If the virtual effective address is equal or greater, a PE occurs.

Before executing a command to transfer control, the processor compares the A address to the current contents of the LAR. If the A address is equal to or greater than the current LAR value and the conditions for transfer of control are satisfied, a PE occurs and the control register for the program remains unaltered. If the A address is smaller than the current LAR, or if LAR is equal to zero, the command execution proceeds normally.

- BAR Addition

After selection of the proper BAR, the contents of the BAR are added to the appropriate bits of the virtual effective address. The sum of the two is the absolute address for the memory access. Bits 24, 23, 22, 21, and 20 of the virtual effective address do not participate in the BAR addition. A carry out of the 22nd bit position of the absolute address causes a PE.

The following illustration shows how an absolute address is obtained from the addition of the virtual effective address and the contents of BAR.



* The decrementing feature of addressing causes the value of the 16th bit of the partial address to be added to the 17th through the 22nd bit positions of the index register contents when forming the virtual effective address.
** If either bit 23 or 24 is equal to 1, a PE results.
*** BAR selector bits for BAR 1, 2, and 3.

- Write Prohibit and Segment Unavailable Flag

  Prior to memory access (after the LAR check and BAR addition), a check is made of the Write Prohibit Flag and the Segment Unavailable Flag for that particular segment of memory. If an attempt is made to write into a segment whose Write Prohibit Flag is on, the access is prevented and a PE occurs. If an attempt is made to access (read or write) a segment whose Segment Unavailable flag is on, the access is prevented and a PE occurs.

Effects of BAR/LAR in User State

In the user state (S-flag OFF), command setup and execution is subject to BAR/LAR processing.

Effects of BAR/LAR in Supervisor State

In the supervisor state (S-flag ON), BAR/LAR processing is dependent on two hardware flags: Flag A, for the A value, and Flag B, for the B value.

If, during the setup phase, the RA character of the command refers to an index register from 1 through 31, Flag A is set ON; otherwise, Flag A is set OFF. If Flag A is set ON, the index register referred to in the RA portion of the command is a user index register relative to BAR X. RA characters obtained by mode 1 indirect addressing have no effect on Flag A. The control of Flag B is identical to that of Flag A, except that the values from the B portion of the command are used.

All memory references by the A or B values, including those derived by indirect addressing, are subject to BAR/LAR processing if the associated Flag A or Flag B is on. If the pertinent flag is off, BAR/LAR processing does not take place for that value.

The following special locations are addressed as absolute index registers. regardless of the state of the A and B flags.

- The Repeat Counter in IR 8, used by the REPEAT command.
- The Jump Link Register in IR 8, stored by the JUMP command.
- The Next Address Index Register in IR 9, stored by the DECODE and SCAN commands.
- The Count Counter in IR 16, used by the COUNT command.

The following trapping flows transfer control to an absolute address, regardless of the state of the S-flag.

- Program Interrupt Trapping Flow
- ME Trapping Flow
- PE Trapping Flow
- Command Code Trapping Flow
- Trace Trapping and address monitoring through the use of the Monitor Register

The S-flag has no effect on the I/O flows.

When the system is powered up, the contents of BAR/LAR registers are indeterminate. BAR/LAR registers are set to their proper values as programs are loaded.

LOAD BAR Command

The processor must be in the supervisor state to execute the LOAD BAR command. The A operand address of the LOAD BAR command specifies one-byte location containing a register indicator. The register indicator specifies which BAR/LAR register is to be loaded with the contents of a 4-byte area specified by the B portion of the command.

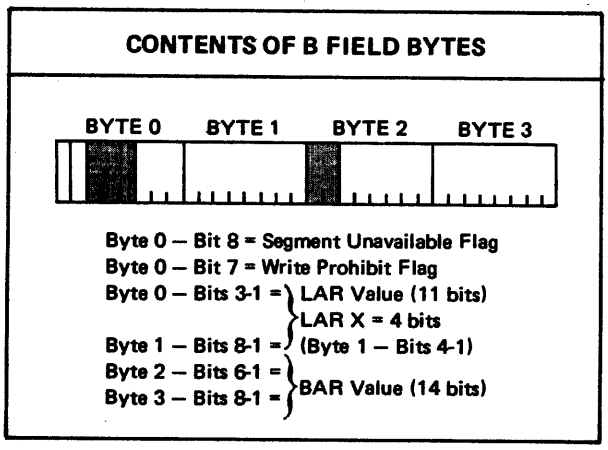
The following illustration shows the bit configuration of the register indicator (A operand) and the BAR/LAR that each specifies.

REGISTER INDICATOR*

Bit Configuration								Specified BAR/LAR
b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	
0	0	0	0	0	0	0	0	BAR/LAR 0
0	0	0	0	0	0	0	1	BAR/LAR 1
0	0	0	0	0	0	1	0	BAR/LAR 2
0	0	0	0	0	0	1	1	BAR/LAR 3
1	0	0	0	0	0	0	0	BAR/LAR X

* Bit configurations other than the ones shown constitute an illegal A operand and result in a PE.

The B operand address in the LOAD BAR command specifies a 4-byte location that contains the values for BAR, LAR, Write Prohibit Flag, and Segment Unavailable Flag.



If the B address is not zero modulo four (0 mod 4), a PE results and the BAR/LAR registers remain undisturbed. If the processor is in the user state (S-flag OFF), the Command Code Trap is taken.

T in the LOAD BAR command is not used; however, for programming compatibility it should always equal zero.

INPUT-OUTPUT CONTROL (IOC)

INTRODUCTION

The design objectives of the NCR Century 300 input-output structure are:

- To provide efficient handling of high-speed peripherals.
- To provide easy expansion into multiple degrees of simultaneous operation.
- To provide multiplexing for several character-level peripherals.

To accomplish these three objectives, the Input-Output Control (IOC) has various trunk controls, a data control section with a direct access to memory, and a selection control. The IOC includes logic, buffering, and multiplexing controls that permit it to operate independently of the ALP once an I/O operation has been initiated.

In the NCR Century 300 the ALP initiates an I/O operation by executing an INOUT command. After the ALP initiates peripheral selection on one of the system's trunks, the proper response from the peripheral unit frees the ALP to return to processing the next program instructions, which may be to issue another INOUT command for a different peripheral. When the ALP completes the selection of the desired peripheral, the IOC assumes control of memory/peripheral communications.

I/O TRUNK CONFIGURATION

There are two I/O trunk configurations in the NCR Century 300; a standard and an optional I/O trunk configuration. The standard configuration consists of six 4-position trunks and one 8-position multiplexor trunk (trunk 0). The optional configuration consists of the standard configuration and four additional 8-position trunks.

All trunks, which carry both control and data information to and from peripherals, contain separate control and data lines.

Common Trunk Concept

The input-output trunk provides communication lines between the processor and the peripherals, both for data and control. The term common trunk means that the processor communicates with all peripherals on a trunk in the same way. The common trunk communication is made possible by a common trunk interface in each peripheral.

The common trunk provides a wide range of input-output facilities for batch and real-time applications. The IOC can accommodate a maximum of 18 I/O operations simultaneously.

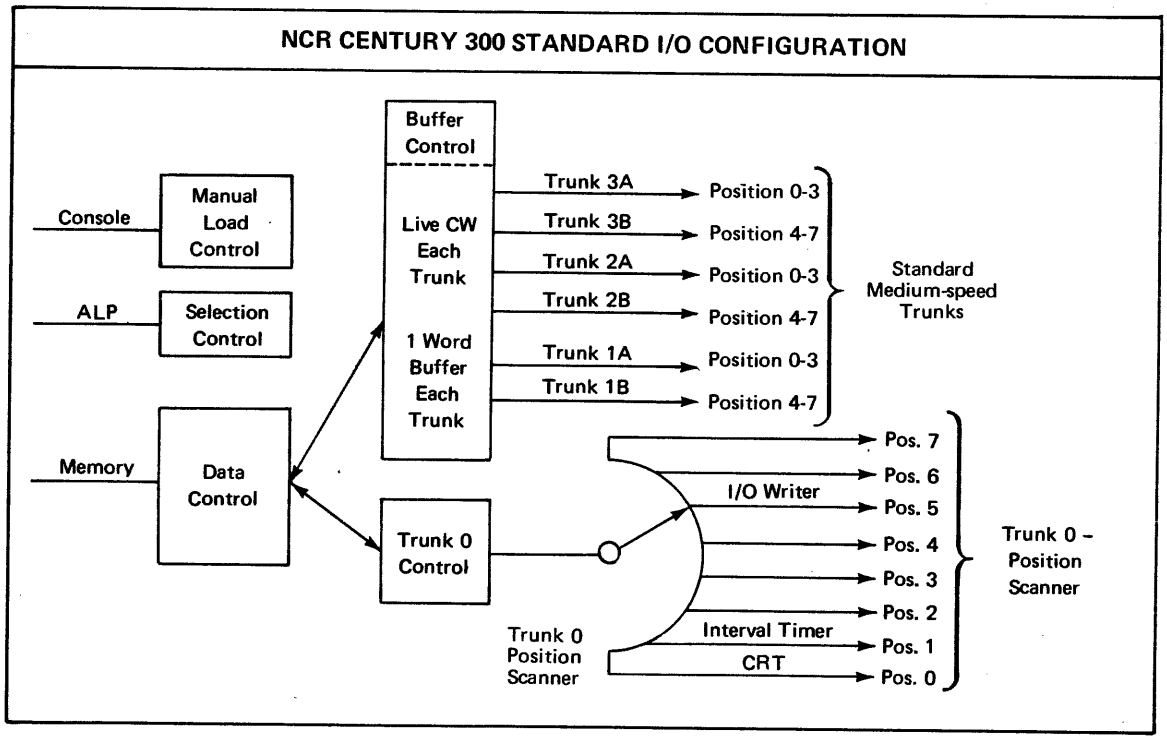
Trunks

- 4-Position Trunks

  In the NCR Century 300, three 8-position trunks were effectively halved, thereby giving the system six trunks of four positions each. Because peripheral units can be active on all trunks simultaneously, the 4-position, 6-trunk design permits up to six simultaneous operations.

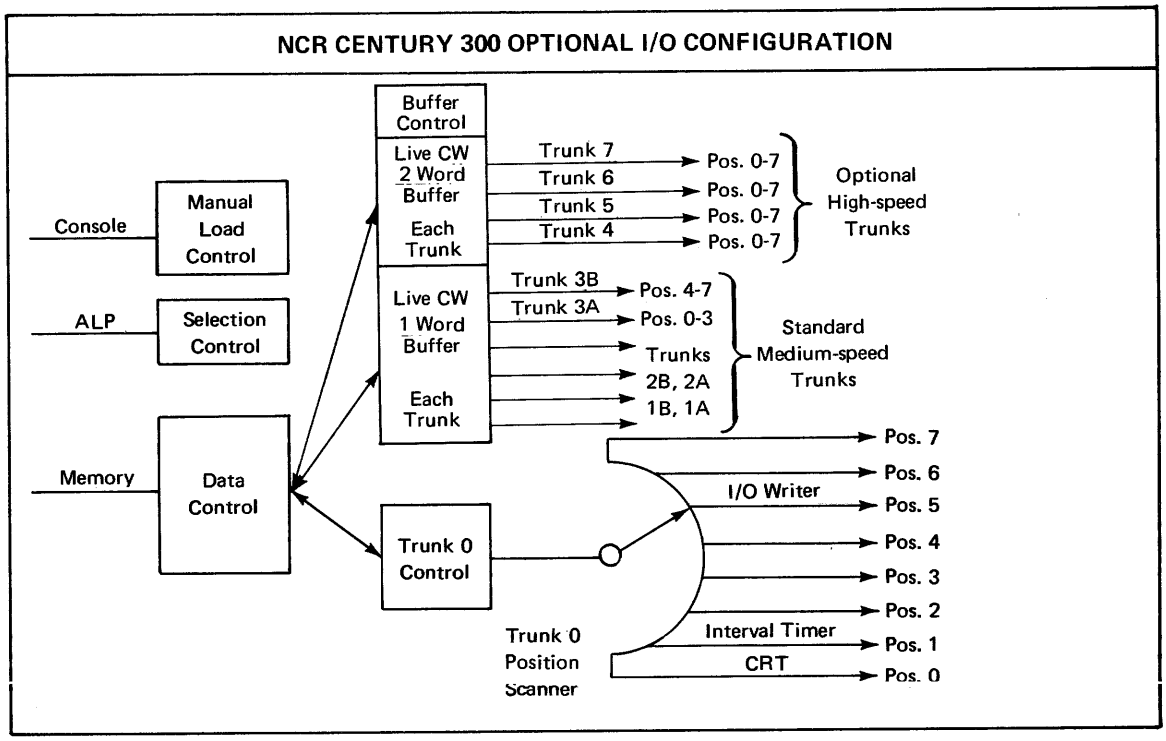
- Multiplexor Trunk

  The 8-position multiplexor trunk, which is time-shared by up to eight peripheral units, transfers data between the IOC and the peripherals one byte at a time. Three of the trunk's positions are dedicated to integrated peripherals. The multiplexor trunk is designed for use with low volume devices (such as the operator's CRT) or low speed devices whose transfer rates are far below the system's capabilities. The IOC constantly scans the positions of the multiplexor trunk and services any active position. Thus, all eight positions appear to have exclusive and simultaneous access to the IOC.



- 8-Position Trunks

An NCR Century 300 System equipped with the optional I/O feature has four additional trunks. Each of these four trunks has eight positions available for peripheral connections.



- Trunk Transfer Rates

The maximum data transfer rate of each 4-position trunk is 815 KB (815,000 bytes per second).

The maximum transfer rate of trunk 0 (multiplexor trunk) has two values: one value, obtained with only 1 active peripheral on the trunk, and another value, obtained with all positions of the trunk active. With only one peripheral active, in addition to the normal transfer time, time is consumed by the multiplexing logic, memory contention, and the turn-around-delay; therefore, although the theoretical transfer rate is 180 KB, the actual permissible transfer rate is 120 KB (120,000 bytes per second).

With all positions active on trunk 0, the same devices do not transfer data consecutively and the turn-around-delay time is eliminated. This reduces the total transfer time and the transfer rate of trunk 0, with all positions active, is 197 KB (197,000 bytes per second).

The maximum data transfer rate of each optional 8-position trunk is 1040 KB (1,040,000 bytes per second).

- Trunk Buffers

  Incorporated in the IOC are buffers for each trunk except trunk 0. These buffers are live registers that are used for temporary data storage. Each of the six 4-position trunks has a 1-word input and a 1-word output buffer. Each of the four 8-position trunks has a 2-word input and a 2-word output buffer. In addition to the buffers, each trunk, except trunk 0, uses a live register for control word storage (refer to "Control Word" in this chapter).

- Trunk Priorities

  The trunk priority during data transfer is in the following sequence: trunk 3A - 3B - 2A - 2B - 1A - 1B - 7 - 6 - 5 - 4 - 0. For example, if trunks 3A and 1A request service simultaneously, trunk 3A is serviced before trunk 1A.

Control and Data Lines

The NCR Century 300 IOC uses separate control and data lines to communicate with the peripherals. The separation of these lines makes it possible to access a control unit (level 1 peripheral) for the purpose of selecting a level 2 unit, although data is being transferred on another level 2 unit. For example, a disc control unit, which controls multiple disc drives, is in the selected state with data being transferred to or from one of the discs. If the ALP tries to select another peripheral on that trunk, it detects the unconditional busy signal and terminates the I/O command execution. The ALP stores an S2 status character of "busy" and the desired peripheral is not selected. If the ALP, while executing a subsequent I/O command, tries to select the disc controller, the busy status is suppressed and the ALP is able to access the idle (not transferring data) disc drives to initiate a seek (locating the proper track, cylinder, and head number) function. The ALP may select the disc controller and issue seek functions to as many as seven disc drives while one is transferring data.

Control Line Parity

To ensure accuracy in transmitting the control characters and to guard against selecting a wrong peripheral unit, all control characters use an accompanying odd parity bit that is generated by the transmitting unit and checked by the receiving unit. Parity bits are used with control characters in selection of a peripheral, acknowledgement (answer-back) by the peripheral, service requests by the peripheral, I/O terminating signals by either the IOC or the peripheral, and transmission of status characters to indicate the outcome of the I/O operation.

Data Handling and Buffering

Data is transferred serially-by-byte between the IOC and the peripheral unit. During input, the IOC checks each character for correct parity. During output, the peripheral unit or its control unit checks each character for correct parity.

Data is transferred parallel-by-word between the IOC and memory through a 4-byte (32 data bits and 4 parity bits) memory port dedicated to the IOC. During input, the IOC generates a parity bit for each byte. During output, the IOC checks the parity of each byte.

During input, each byte from a peripheral unit is stored in the buffer of the IOC until a complete word is received; the word is then written into memory. During output, one complete word is read from memory into the buffer of the IOC and then sent serially-by-byte to the peripheral.

On all buffered trunks, four bytes are transferred for each memory cycle. On trunk 0, however, four memory cycles are required for each byte input or output. These cycles are necessary because trunk 0 data transfer occurs one byte at a time. Since data is multiplexed, each byte may be received from, or sent to, a different peripheral unit. Therefore, there is neither a buffer nor a live register for the control word in the trunk 0 control.

Bandwidth

The activities that take place in a computer system during processing occur at varying rates of speed. The term bandwidth is defined as the maximum number of bytes that can be transferred in one second.

In the NCR Century 300 the maximum bandwidth at which I/O transfers can occur is 3720 KB.

Peripheral Types

NCR Century series peripherals are classed as either integrated peripherals or freestanding peripherals.

- Integrated Peripherals

  Three integrated peripherals are incorporated in the NCR Century 300 System: the I/O Writer, the operator's CRT Display, and a non-addressable Interval Timer. (See "Interval Timer" in this chapter.)

  All integrated peripherals in the NCR Century 300 System share the logic and power supplies of the IOC.

- Freestanding Peripherals

  Freestanding or common trunk peripherals are used interchangeably to indicate the same thing. A freestanding peripheral may be connected to any I/O trunk at any position not reserved for integrated peripherals, provided the data transfer rate of the peripheral does not exceed the data transfer rate of the trunk.

  Freestanding peripherals are classified as either level 1 or level 2.

  - Level 1 Peripherals

    A level 1 peripheral, occupying a position on an I/O trunk, contains its own control logic for communication. There may be as many level 1 units on a trunk as the trunk has positions.

  - Level 2 Peripherals

    Level 2 peripherals interface to the I/O trunk through a control unit or multiplexor. During I/O operations, the IOC communicates with the control unit which supervises the actual peripheral operation through another

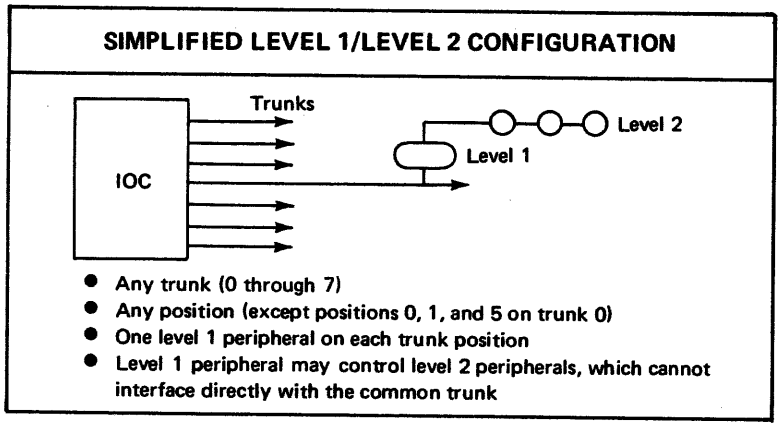
trunk that is similar to the I/O trunks. The controller is a level 1 unit; the peripheral units connected to the controller's trunk are level 2 peripherals.

The unit selection character (8 bits) can specify up to 256 level 2 peripherals. The actual number of peripherals that may be used depends on the level 1 device controlling the level 2 devices; however, 256 is the maximum.

- Additional Level Peripherals

  Additional levels of peripherals are permissible. Each new level requires an additional selection character (8 bits) permitting up to a maximum of 256 selectable devices.

In the following illustration, one level 1 peripheral (in this case a control unit) is connected directly to a trunk, and three level 2 units are connected indirectly to the same trunk and position number through the single level 1 control unit.



FUNCTIONAL OPERATION

The three phases of the I/O operation -- selection, data transfer, and termination -- are discussed in this section.

Selection

An I/O operation is initiated when the ALP selects a peripheral by executing an INOUT command. Selection includes selecting a peripheral, initiating the desired function (read, write, print, etc.), and issuing any special instructions required by the specified peripheral.

- INOUT Command

  The INOUT command may be a single- or double-stage command. The single-stage INOUT command loads the I/O control unit priority register. A double-stage INOUT command selects and initiates an I/O function in a peripheral unit. For a detailed explanation of the INOUT command, refer to the "NCR Century 251/300 Hardware Commands," under this tab.

- Peripheral Address Field (PAF)

The effective A portion of the INOUT command specifies the address of the Peripheral Address Field (PAF). The PAF contains all information necessary -- the trunk and position characters, the unit character if applicable, and the function character -- to complete an I/O selection operation.

Since some peripherals require more information than others, the PAF is a variable-length field. For example, a paper tape reader can only read; therefore, it is only necessary to select the reader to initiate its function. Peripherals such as magnetic tape units, which perform more than one function must be selected and told what specific operation to perform. In this case the PAF must be longer than the minimum length of 1 byte.

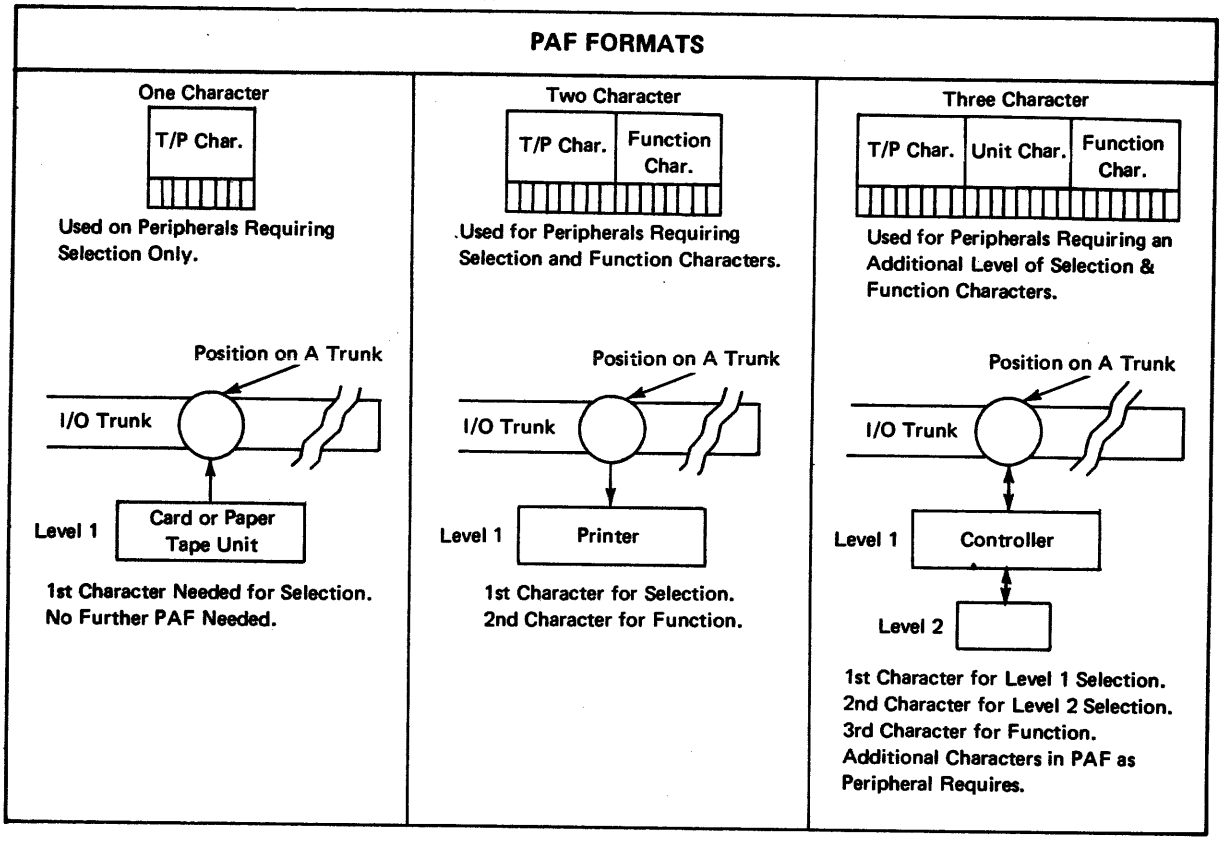
The first character of the PAF contains the trunk number (T) and position number (P) as illustrated below:

T/P CHARACTER FORMAT

b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	T	T	T	0	P	P	P

TTT = I/O trunk number (0 through 7)
PPP = Position number (0 through 7)

In the NCR Century 300 System, b8 and b4 are 0 for compatibility with other NCR Century systems. The arrangement of the PAF characters following the T/P character is determined by the functional characteristics of the peripheral. Level 1 peripherals that perform more than one function, but which need no additional addressing, require a function character following the T and P character. Control units require a unit character in the PAF to select a level 2 peripheral connected to the control unit.



S2 Status Character

The S2 status character reflects the results of an attempt to select and activate the peripheral unit designated by the PAF. The B portion of the INOUT command specifies the memory location where the ALP is to store the S2 status character before terminating the INOUT command.

The ALP generates the S2 status character based on the answer-back signals it receives from the peripheral during the selection process.

After storing an S2 status character, the ALP returns to internal processing operations, leaving the IOC to supervise data transfer.

The seven possible S2 status characters and their binary and hex configurations are:

- PAF Parity Error (10100011) (A3)

  Either the IOC or a level 1 peripheral detects a parity error on the control information lines. The parity error, if detected by the IOC, is present in the selection character from the ALP; if detected by the level 1 peripheral, the parity error is present in the selection character from the IOC. When the error is detected, the IOC notifies the ALP to that effect and the ALP stores the PAF Parity Error S2 status character.

- T/P Miscompare (10100100) (A4)

  In addition to the T/P (trunk and position) number specified in the first PAF character, the ALP sends the T/P number to the IOC by the trunk/position interface lines, with each PAF character, to aid in the selection process. If the IOC detects a difference between the information in the T/P interface lines and the corresponding T/P number of the first PAF character, it notifies the ALP to that effect and the ALP stores the T/P Miscompare S2 status character.

- PAF Parity Error & T/P Miscompare (10100111) (A7)

  If the IOC detects this multi-status error, it notifies the ALP to that effect and the ALP stores the PAF Parity Error & T/P Miscompare S2 status character.

- Busy (10000000) (80)

  The busy indication means either that the I/O trunk is servicing another peripheral or that the selected peripheral itself is busy. However, common trunk control units for CRAM or disc can share seek time (the time required to locate the track where information is to be stored or read). Thus, the control unit for these peripherals can suppress the busy status to permit a seek operation even when another peripheral in the controlled group is engaged in an I/O operation.

- Standby (10000010) (82)

  When the STOP switch on a peripheral console is pressed (to permit changing of a disc, for example) prior to peripheral selection, the peripheral is placed in standby, and the ALP stores the Standby S2 status character.

- Inoperative (00000010) (02)

  Two conditions cause the ALP to store an Inoperative S2 status character: the peripheral is not responding to selection within the allotted time (a response error), or the peripheral is physically inoperative because the USE LOCKOUT switch is ON, the peripheral is out of media, etc.

- Command Initiated (01000000) (40)

  This configuration is stored as soon as the selected peripheral has accepted all PAF characters.

- S2 Priorities

  The processor stores the S2 status characters according to a pre-determined order of priority because more than one S2 status character condition may result, but the ALP can store only one S2 status character to reflect the result of a selection attempt.

The following table lists the S2 status characters in the order of their priority.

S2 STATUS CHARACTER PRIORITY

Priority	Bit Configuration		Status
	Binary	Hex	
1	1000 0000	80	Unconditional Busy
2	1010 0011	A3	PAF Parity Error
3	1010 0100	A4	T/P Miscompare
4	1010 0111	A7	PAF Parity Error & T/P Miscompare
5	1000 0000	80	Conditional Busy
6	1000 0010	82	Standby
7	0000 0010	02	Inoperative
8	0100 0000	40	Command Initiated

NOTE

An integrated peripheral may cause the processor to store an S2 Busy status character if the device is still performing the previous function although an S3/S4 status character may have been already stored for that function. For example, the ALP stores an S2 Busy status character for touchplate selection if any of the touchplate switches are still pressed from the previous selection.

Data Transfer

When the selected peripheral is ready to receive or transmit a character of data, it sends a request for service to the IOC. When this request is received, the IOC accesses memory to read out or store the data.

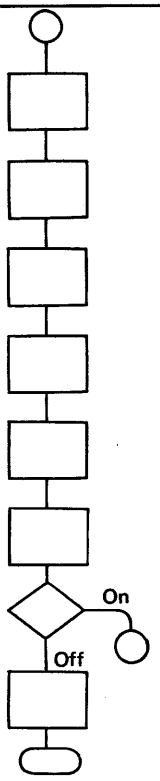
A peripheral unit on trunk 0 accompanies each request for service with a response number. The IOC uses the response number to calculate the memory address of the control word (CW) for the designated peripheral. Trunks 1B through 7 have "live" control words, directly updated by the IOC, to reduce the memory accesses during I/O operations and to permit higher transfer rates. (Control words are explained later in this chapter under "Control Word.")

During an input operation, trunks 1 through 7 transfer data to their respective buffers serially by byte until the buffer is full. (Trunks 1 through 7 utilize live buffers.) The IOC stores the contents of the buffer, one word (4 bytes) at a time, in the memory location specified by the control word. For data output, data is transferred from memory to the buffer, one word (4 bytes) at a time, and then serially by byte to the selected peripheral unit.

Since trunk 0 has no buffer, nor a control word in the IOC, each byte that is input or output requires four memory cycles (2 cycles to read out the 8-byte control word, 1 cycle to read or write one byte of data, and 1 cycle to restore the incremented "next address" portion of the control word in memory).

The following two flow charts are simplified descriptions of the IOC operation. The first flow is for trunk 0, and the second flow is for trunks 1 through 7.

TRUNK ZERO I/O CONTROL OPERATION



Start

Peripheral requests service, sends response number

I/O control accesses memory

NA supplies the data address to be used

Increment NA by 1

If NA = TA, set flag

If output mode: Read out character and send to peripheral
If input mode: Store character received from peripheral

Test flag

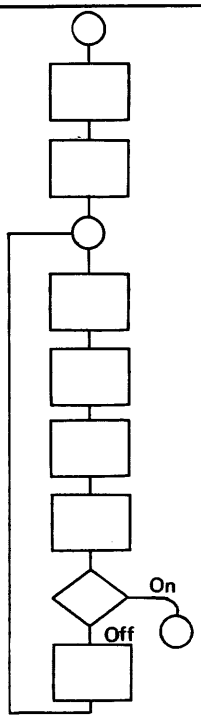
Go to priority interrupt and termination queue routine

The I/O control waits for next request for service

Start

This flow chart is a simplified description of I/O control operation during data transfer. It is not intended as a programming guide.

TRUNK 1 TO 7 I/O CONTROL OPERATION



Start

Peripheral requests service, sends response number

IOC accesses memory, stores NA and TA in live registers

NA supplies the data address to be used

Increment NA by 1

If NA = TA, set flag

It output mode: Read one word of data from memory, load into buffer, and transmit to peripheral, one byte at a time

If input mode: Fill buffer, one byte at a time, from peripheral and write into memory, one word (4 bytes) at a time

Test flag

Go to priority interrupt and termination queue routine

This flow chart is a simplified description of I/O control operation during data transfer. It is not intended as a programming guide.

- Response Number

Each common trunk peripheral unit has an 8-bit response number wired into its logic circuitry. When a peripheral unit requests service from the processor, the response number accompanies the request. The IOC uses this number to compute the starting address of the control word. Control word addresses begin at memory location 1024 (decimal). To calculate the CW address, the IOC multiplies the response number by 8 (each control word contains 8 characters) and adds the results of the multiplication to 1024.

EXAMPLE:

To calculate the CW address when the response number is 5:

1. 5 x 8 = 40
2. 1024 + 40 = 1064

Response number 5 indicates CW 5. The starting address of CW 5 is 1064.

NOTE

> Once the control word address is calculated for a unit on trunks 1B through 7 and the CW is stored in the live register, no further use is made of the response number until the CW is returned to memory at termination of the I/O operation. For this reason, devices (such as a communications multiplexor) which transfer data to various control words between terminations, must be assigned to trunk 0.

- Control Word

A control word (CW) is an 8-byte field containing such information as the priority of the active peripheral, the current address of the data being input or output, the final address to be accessed, and certain status characters. The NCR Century 300 can accommodate 256 control words. As an option, positions 3 and 4 of trunk 0 can be wired, at the time of installation, to provice an additional 256 control words. The maximum number of control words is 512.

Of the two types of control words used in the NCR Century 300, all peripherals, except the printer, use a standard control word. The printer uses a different type, unique only to printer operations. For a description of the printer control word, refer to the PRINTERS tab, in this manual.

The following illustration shows the format and contents of a standard control word.

STANDARD CONTROL WORD FORMAT

S/P	NA			TA		2-Character Area Reserved for Software Use
	N3	N2	N1	T2	T1	

S/P = A 1-character field containing the priority number of the peripheral unit. At termination, the S3 or S4 status character is stored in this location.

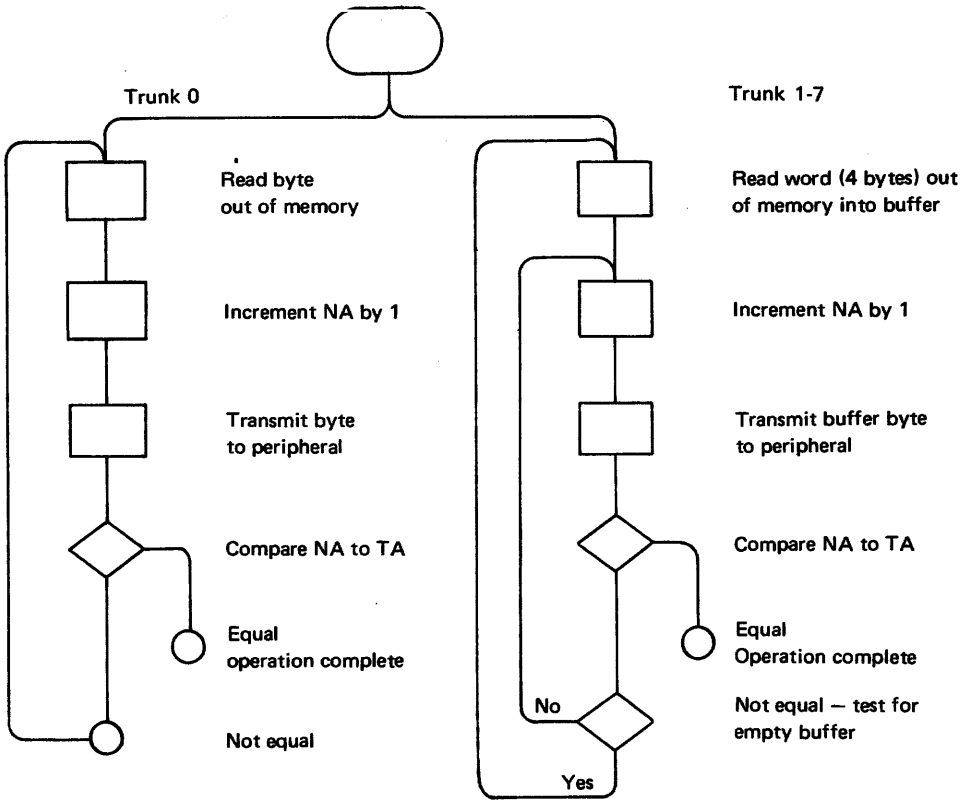
NA = A 3-byte binary field containing the next memory address to be accessed by the IOC for output, or storage, of data.

TA = A 2-byte binary field containing the terminating address. TA is compared to the N2 and N1 characters of the NA field to determine I/O completion. NA, a 24-bit (3-byte) field, is used in both input and output operations. It provides the address into which the character is stored or from which the character is read. NA is incremented by a binary 1 and the N2N1 characters are compared to the two TA characters (16 bits) which always contain the last address +1 of the data storage areas. Comparing NA to TA determines when the processor has arrived at the end of a data field. If they are equal, the operation terminates. This 16-bit comparison permits a theoretical record size in the NCR Century 300 of up to 65,536 characters.

NOTE

Since special action is required of the IOC to align the data within the first and last words of records, the speed of the I/O operation can be increased by making NA equal to 0 modulo 4. This is not a requirement, however.

The following illustration shows the general flow of an output operation and NA/TA comparison.



Termination

Under normal terminating conditions, the IOC ends an I/O operation in a predictable, orderly manner and stores a status character where it is accessible to the operator and/or the program. In general, the status character, which is stored in the first byte of the control word, reflects the outcome and specifies the cause for the termination of the I/O operation.

Termination of an I/O operation may be initiated either by the IOC or the affected peripheral. Termination falls into two categories:

- Processor termination -- Initiated either by the IOC or the peripheral. Peripheral generates an S3 status character and sends it to the IOC, which stores it in the associated control word.
- Latent Error Termination -- Initiated only by the IOC, which inhibits the peripheral from sending an S3 status character. Instead, the IOC generates an S4 status character and stores it in the associated control word in place of the S3 status. In special cases, a substitute character may be stored in lieu of an S4 status character, as explained later, under "Response Number Parity Error."

The above two major categories may be divided into four specific types of termination, which are explained next in more detail.

- Normal Processor Termination

  The IOC sends a terminate signal to the peripheral when the incremented NA = TA in the control word. In turn, the peripheral sends its response number and an S3 status character to the IOC.

  Upon receipt of a processor terminate signal, a real-time, level 1 peripheral (such as a communications adapter) replies by sending an S3 Segment Complete status character to the IOC. Before further communication with that peripheral can occur, the processor must issue another read or write function. If a character is received at the controlling device before a read or write function is issued, a Program Overload occurs.

  Other peripherals (not real-time) continue reading until they detect an end-of-block (EOB) condition (end-of-card, end-of-sector, record gap, special character, etc.) before stopping and sending the appropriate S3 status character to the IOC. A peripheral that does not detect an EOB condition (for example, paper tape reader) stops reading immediately upon receipt of the termination signal and sends the appropriate S3 status character to the IOC.

  When a peripheral receives the processor termination signal while writing, the peripheral initiates an EOB write operation before terminating the write operation and sending the appropriate S3 status character to the IOC. A peripheral that does not initiate an EOB write operation (for example, paper tape punch) stops writing (punching) immediately upon receipt of the termination signal and sends the appropriate S3 status character to the IOC.

- Normal Peripheral Termination

  If a peripheral detects an EOB condition before a processor terminate signal is received, the peripheral requests service and sends a termination signal with the appropriate S3 status character to the IOC. The IOC stores the status character in its proper memory location and terminates the I/O operation.

- Special Peripheral Termination

  When the peripheral detects any of the following conditions, it immediately sends a terminate status signal with the appropriate S3 status character to the IOC:

  - Error when writing
  - System overload when writing
  - Write lockout when attempting writing, erasing, or rewinding (Rewinding is initiated; writing and erasing are not.)
  - Inoperative, when executing any function
  - Transmission errors
  - Other exception conditions, e.g., error when reading from bit-serial magnetic media such as discs.

  Other conditions that are detected by the peripheral but are usually not transmitted to the IOC until an EOB condition is detected or until the next INOUT command is initiated are:

  - Error when reading (EOB)
  - System overload when reading (EOB)
  - Program overload (next INOUT command)

- Special Processor Termination

  If the IOC terminates an I/O operation because of a Latent Program Error (LPE), a Latent Memory Error (LME), a Latent Transmission Error (LTE), or an IOC Buffer Parity Error, it inhibits the peripheral from sending an S3 status character. Instead, the IOC generates and stores an S4 status character in place of the S3 status character.

Termination Flow

The NCR Century 300 employs a priority technique to determine whether a terminating peripheral may interrupt the central processor. The processor and each peripheral are assigned priority numbers by the user program. The processor's priority number is stored in a 4-bit register (Priority Register) in the IOC; each peripheral's priority number is stored in its control word.

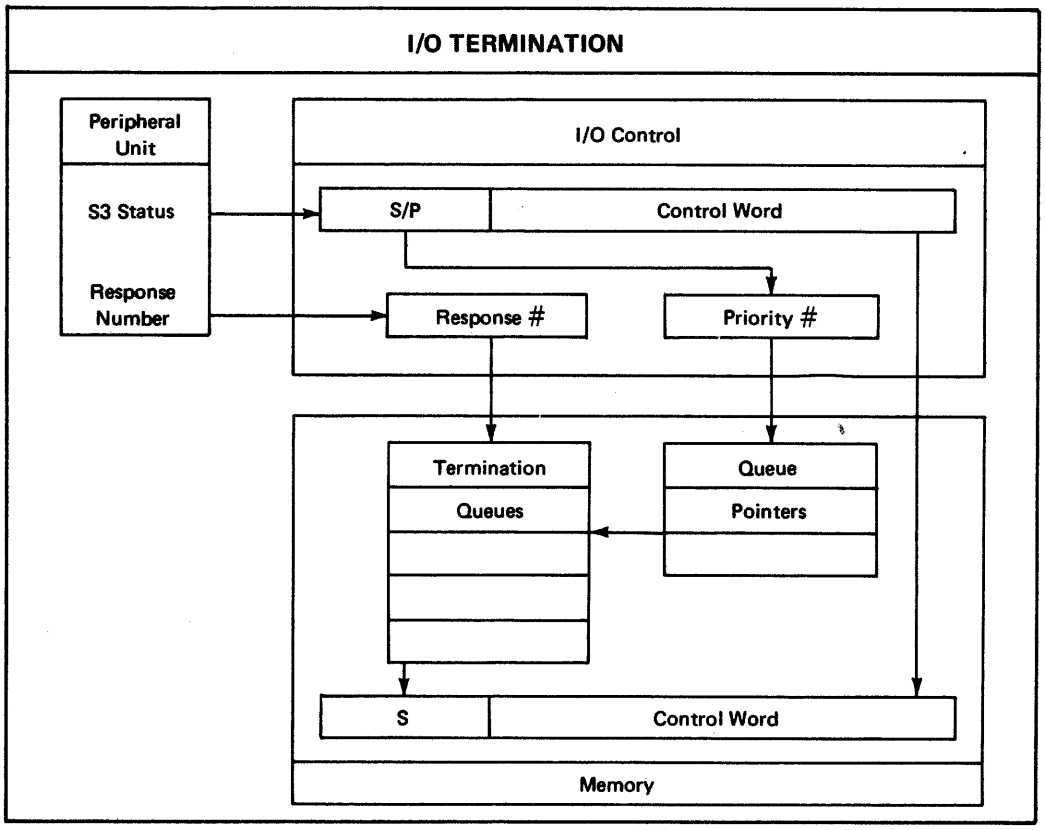
Upon termination the peripheral unit sends its response number and status character to the IOC. The IOC saves the least significant four bits of the S/P byte (Priority Level number) of the Control Word for later use. The IOC stores the S3 status character in the S/P byte of the Control Word, calculates the memory address (according to the response number received from the peripheral) and stores the control Word contents at this address.

For each of the 16 interrupt priority levels, the IOC maintains a cyclic 256-byte queue in memory. The IOC stores the response number of the interrupting peripheral in the termination queue corresponding to the interrupt priority level assigned to that device for that specific operation. The termination queues are addressed by termination queue pointers. There is a termination queue pointer for each termination queue. Each pointer is a 4-byte area whose least significant 18 bits contain the address of the next entry position in the termination queue. Using the priority number saved from the Control Word, the IOC calculates the location of a termination queue pointer. The pointers start at memory location 384. IOC calculates their addresses according to the following scheme:

CALCULATION OF TERMINATION QUEUE POINTER ADDRESSES
Priority Number x 4 + Beginning Address = Termination Queue (384) Printer Location

Peripheral priority number 15 represents the highest priority; priority number 0 represents the lowest priority.

The IOC adds 1 to the least significant byte of the termination queue pointer each time it makes an entry in the termination queue. Since no carry is propagated out of the low order byte of the address, the termination queue is cyclic 256. Each time the IOC makes an entry in the termination queue, it also sets bit 8 of the most significant byte (bit 32) of the pointer to 1 as an indicator to the processor that activity has occurred in that queue.



Next, the IOC compares the interrupt priority number to the processor's priority number which is stored in a special 4-bit register. If the interrupt priority is equal to or lower than the processor's priority, no action is taken at this time. If the interrupt priority is higher than the processor's priority, the Interrupt Indicator (II) is turned on to signify that a priority interrupt condition exists. If the Interrupt Permit (IP) is ON, the processor traps out of the normal program flow to a subroutine in which it examines bit 32 of each termination queue pointer. If bit 32 is OFF, the processor moves to the next pointer in the list. If bit 32 is ON, the processor uses the pointer to locate the peripheral response number, calculates the location of the control word, and takes the course of action specified by the S3 status character which is stored in the S/P byte of the Control Word. This routine is repeated until all terminations have been processed. System software then resets the termination queue pointers, determines the highest priority program to be run, resets the processor priority number accordingly, and reenters the program flow.

S3 Status Character

The processor generates and stores an S2 status character to indicate the results of attempted peripheral selection. At termination of an I/O operation, a similar 8-bit character, called an S3 status character, is generated by the peripheral unit and sent to the IOC, which stores it in the first byte of the control word. This character reflects the outcome of the I/O operation. After a processor interrupt occurs, system software examines this status character and takes the appropriate action. If an error occurs during the I/O flow, the IOC inhibits the peripheral from sending an S3 status character. Instead, the IOC generates an S4 status character and stores it in place of the S3.

The S3 character has 10 possible configurations and meanings. If bit 8 and bit 7 are both 0, the I/O operation is complete; if bit 8 and bit 7 are both 1, the transfer of one segment of data has been completed. If only bit 8 is ON, the operation has been terminated early due to a transmission error or operator instruction. Although the peripheral may send only one S3 status character to the IOC, the bit configuration of that character may reflect more than one condition, provided they are not mutually exclusive.

The following S3 status character definitions, which include their binary and hex configurations in parentheses, are general in nature. Certain peripherals have specific status characters that are explained in the separate publications dealing with these devices.

- Operation Complete (00XXXXXX) (00)

  This configuration is stored when the I/O operation is complete. Errors and exceptions encountered during the operation are indicated by various combinations of b6 through b1.

- Segment Complete (11XXXXXX) (C0)

  This configuration indicates that processor termination occurred while a real-time peripheral had more data to transmit to its control unit. The processor must reissue a read function to activate the remote peripheral. If a data character arrives at the control unit before the function code, a Program Overload occurs.

- Error (00100000) (20)

  This configuration occurs when the selected peripheral detects an error (usually a parity error) during an I/O operation. If the error is detected while the peripheral is performing a read operation, the error is noted and sent as a bit in the S3 status character configuration when the terminating status is sent. If the error is detected while writing, a terminating status signal and the proper S3 status character are sent to the processor immediately.

- System Overload (00010000) (10)

  When the IOC does not respond to the selected peripheral's request for service within the character time, the peripheral unit detects a system overload. Character time, the amount of time required for a peripheral to receive or transmit 1 byte of data, varies with the peripheral unit. Data transmission ceases when a system overload is detected.

  If the peripheral unit detects a system overload during a write operation, it sends a terminating signal and the appropriate S3 status character to the IOC immediately. If a system overload is detected during a read operation, the peripheral notes the condition and sets the proper bit in the status character when a terminating status is sent.

- Media (00001000) (08)

  This configuration is stored when the selected peripheral detects a warning marker, such as a magnetic tape destination warning marker, during a write operation. The warning marker is noted and sent as a bit in the S3 status character configuration when the terminating status is sent. The IOC continues data transmission, despite the peripheral's detection of the warning marker, until the processor terminate signal is received.

- Write Lockout (00000100) (04)

  This configuration is stored when the IOC attempts to write in a peripheral which is in the write lockout state (for example, a magnetic tape handler). The elapsed time between S2 and S3 storage, in this case, may be so slight as to be undetectable by the program.

- Inoperative (00000010) (02)

  The inoperative configuration is stored when certain malfunctions (out of media, torn punch tape, etc.) are detected by the peripheral after it has been activated. Data transmission ceases immediately and the terminating status signal, along with the inoperative status character, is sent to the IOC.

- Special (00000001) (01)

  This configuration is stored to indicate any condition not included above. The actual configuration used will depend upon the specific peripheral involved.

- Transmission Error (10000000) (81)

  This configuration is stored if a transmission parity failure is detected by a peripheral during the I/O operation. When a transmission parity error is detected, the peripheral immediately deselects itself and sends this status character.

- Standby (10000010) (82)

  This configuration is stored if the STOP switch on the selected peripheral has been pressed.

During the I/O operation more than one status condition can occur. When the S3 status character is sent to the IOC, multiple status conditions may be combined into a single S3 by logical (mod 2) addition of the corresponding bits of the individual status characters. All, except the mutually exclusive, status conditions may be so combined.

Under certain conditions, caused by malfunctions, an S3 is not sent to the IOC by the affected peripheral unit. These special cases are handled by software, as described next.

- Lost S3 Status

  The IOC employs a control line to constantly monitor the operational condition of a selected level 1 peripheral. This control line is used only with the medium- and high-speed trunks, not the multiplexor trunk. If a malfunction occurs in a peripheral that prevents it from completing the data transfer, or sending an S3 status character, the control line monitoring the peripheral resets (clears) the live control word in the trunk buffer control. The IOC, consequently, does not store status, make an entry in the terminating queue, or store the control word in memory.

  Software detects the incomplete I/O operation when the allocated time for the I/O expires (software timeout) and initiates the appropriate recovery procedure. Software generates a pseudo S3 (hexadecimal 4F) in place of the lost S3 when the timeout occurs.

- NA = TA Error Detection

  When the incremented NA equals TA (NA + 1 = TA), the IOC sends a processor termination signal to the peripheral. The IOC anticipates receiving an S3 status character from the peripheral. Instead, however, the peripheral raises a request for service. When the IOC detects this error condition, it sends a Latent Error signal to the peripheral and deselects it. The IOC resets (clears) the control word, and does not store status, make an entry in the termination queue, or store the control word in memory.

  Software detects the incomplete I/O operation by software timeout and initiates the appropriate recovery procedure.

S4 Status Character

Whenever the IOC detects a latent error condition during an I/O operation, it terminates the I/O operation, deselects the peripheral, and inhibits the peripheral from sending an S3 status character. In place of the S3 status character, the IOC generates and stores in the control word an S4 status character.

A latent error is one detected by the IOC and stored as an S4 status character in the control word in memory.

The four latent error conditions and their corresponding S4 status characters are:

- Latent Program Error (10001000) (88)

  An IOC-detected Program Error (PE) where part or all of the data fields exceed memory size during input or output.

- Latent Memory Error (10000100) (84)

  An IOC-detected memory error (ME) where a parity or other control-code error occurred when being read from memory. The error may occur when the IOC attempts to read data or the NA/TA portion of the control word.

  If the ME occurs while the IOC is reading NA or TA from memory, the NA is not incremented and the data character is not transferred to, or accepted from, the peripheral.

  If the ME occurs while the IOC is reading data from memory, the NA in the control word is updated, but the character is not transferred to the peripheral.

- Latent Transmission Error (10000001) (81)

  An IOC-detected transmission error (TE) is a latent transmission error, where a parity error occurs in an incoming data byte or the S3 status character from a peripheral, or in the data read from memory.

  If a transmission error is detected in the data being read from memory, the character in error is returned to memory with the correct parity.

- IOC Buffer Parity Error (10110000) (B0)

  If a parity error is detected in the data that is output from the trunk buffer, either to memory or to the common trunk, the IOC Buffer Parity Error S4 status character is stored in the control word when the operation terminates.

  This error can occur only during an I/O operation on the medium- and high-speed trunks, not on the multiplexor trunk.

  Multiple status conditions may be reflected in one S4 status character. The following table lists the four primary S4 status characters and all the possible combination status conditions reflected in one S4 status character.

S4 STATUS CHARACTERS		
PRIMARY S4 STATUS CHARACTERS		
Bit Configuration		Status
Binary	Hex	
1000 0001	81	Latent TE
1000 0100	84	Latent ME
1000 1000	88	Latent PE
1011 0000	B0	IOC BE
COMBINATION S4 STATUS CHARACTERS		
Bit Configuration		Status
Binary	Hex	
1000 0101	85	TE and ME
1000 1001	89	TE and PE
1000 1100	8C	PE and ME
1000 1101	8D	TE, PE and ME
1011 0001	B1	BE and TE
1011 0100	B4	BE and ME
1011 0101	B5	BE, TE and ME
1011 1000	B8	BE and PE
1011 1001	B9	BE, TE and PE
1011 1100	BC	BE, PE and ME
1011 1101	BD	BE, TE, PE and ME

Response Number Parity Error

A request for service by a peripheral is accompanied by a response number. The IOC uses the peripheral's response number to compute the address of the associated control word. The response number is composed of eight bits plus an odd parity bit. The IOC checks the parity of each response number from the multiplexor trunk, but the parity of only the first and the last response numbers from the medium- and high-speed trunks, since these use live registers for control word storage.

If the IOC detects a parity in the response number, a latent response-error condition exists, and the I/O operation is terminated. Because the response number is erroneous, the IOC cannot compute the right control word address. The S4 status character, which is normally stored in the control word in memory, is now not available (non-existent).

As an alternative, in lieu of the nonexistent S4, the IOC stores the trunk number in Termination Queue (TQ) 0, specified by Termination Queue Pointer (TQP) 0. The II is not set ON.

TQP 0 and TQ 0 are reserved for IOC use to store the trunk number where a response number parity error occurred.

The incomplete I/O operation is detected by software timeout and the appropriate recovery procedure is initiated.

The following bit configurations are stored in TQ 0 to indicate the trunk numbers of trunks 1B through 7 and the position numbers of trunk 0, where the response number parity error occurred.

RESPONSE NUMBER PARITY ERROR S4 ALTERNATIVES					
HIGH-SPEED TRUNKS		MEDIUM-SPEED TRUNKS		MULTIPLEXOR TRUNK	
Trunk Number	Bit Configuration	Trunk Number	Bit Configuration	Position Number	Bit Configuration
7	0111 0000	3A	0011 0000	0	0000 0000
6	0110 0000	3B	0011 0100	1	0000 0001
5	0101 0000	2A	0010 0000	2	0000 0010
4	0100 0000	2B	0010 0100	3	0000 0011
		1A	0001 0000	4	0000 0100
		1B	0001 0100	5	0000 0101
				6	0000 0110
				7	0000 0111

INTERVAL TIMER

The integrated interval timer provides the operating system with the ability to interrupt a program after a specified number of milliseconds. Thus, in a multiprogramming environment, the interval timer prevents any program from using more ALP time than specified. By doing this, the timer also detects and prevents program loops.

Functional Operation

The interval timer, occupying position 1 of trunk 0, makes use of certain input-output features in its operation. Every millisecond the timer requests service from the IOC. The IOC reads the NA portion of the control word, increments it by one and compares the incremented NA to the TA portion of the control word. If NA $\neq$ TA, the IOC writes the incremented NA back into the control word and the timer continues to count and raise service requests to the IOC. When NA = TA, an Operation Complete S3 status character is stored in the interval timer's control word and the II is turned ON, unconditionally (no priority check is performed). The interval timer, as a special integrated peripheral, has no response number assigned to it. The IOC calculates the timer's control word address (special control word at memory location 336) by using a pseudo response number. As a result, no activity occurs in the Termination Queue or the Termination Queue Pointer when the interval timer terminates; therefore, software tests the interval timer control word during each interrupt trap routine to see whether the interrupt was caused by the timer or not.

Terminaiton

The interval timer continues to count and raise service requests until one of the following conditions arises: NA = TA, the IOC fails to service a request, the ALP enters the Halt state, or a latent ME is detected.

When NA = TA, an Operation Complete S3 status character (0000 0000) is stored in the control word and the II is turned ON unconditionally.

If the IOC fails to service a request, a System Overload S3 status character (0001 0000) is stored in the control word and the II is turned ON unconditionally. The interval timer raises a service request to the IOC for 750 microseconds. If the request times out without being serviced, a subsequent request that is serviced causes the System Overload status to be stored in the control word.

If the ALP enters the Halt state, a Special S3 status character (0000 0001) is stored in the control word and the II is turned ON unconditionally.

If a latent ME is detected, an S4 status character (1000 0100) is stored in the control word and the II is turned ON unconditionally.

Halt State

The interval timer runs continuously, except when the ALP is in the Halt state. As the ALP enters the Halt state, the Special S3 status character is stored in the control word, the II is turned ON, and the timer stops counting. The timer resumes counting as the ALP leaves the Halt state.

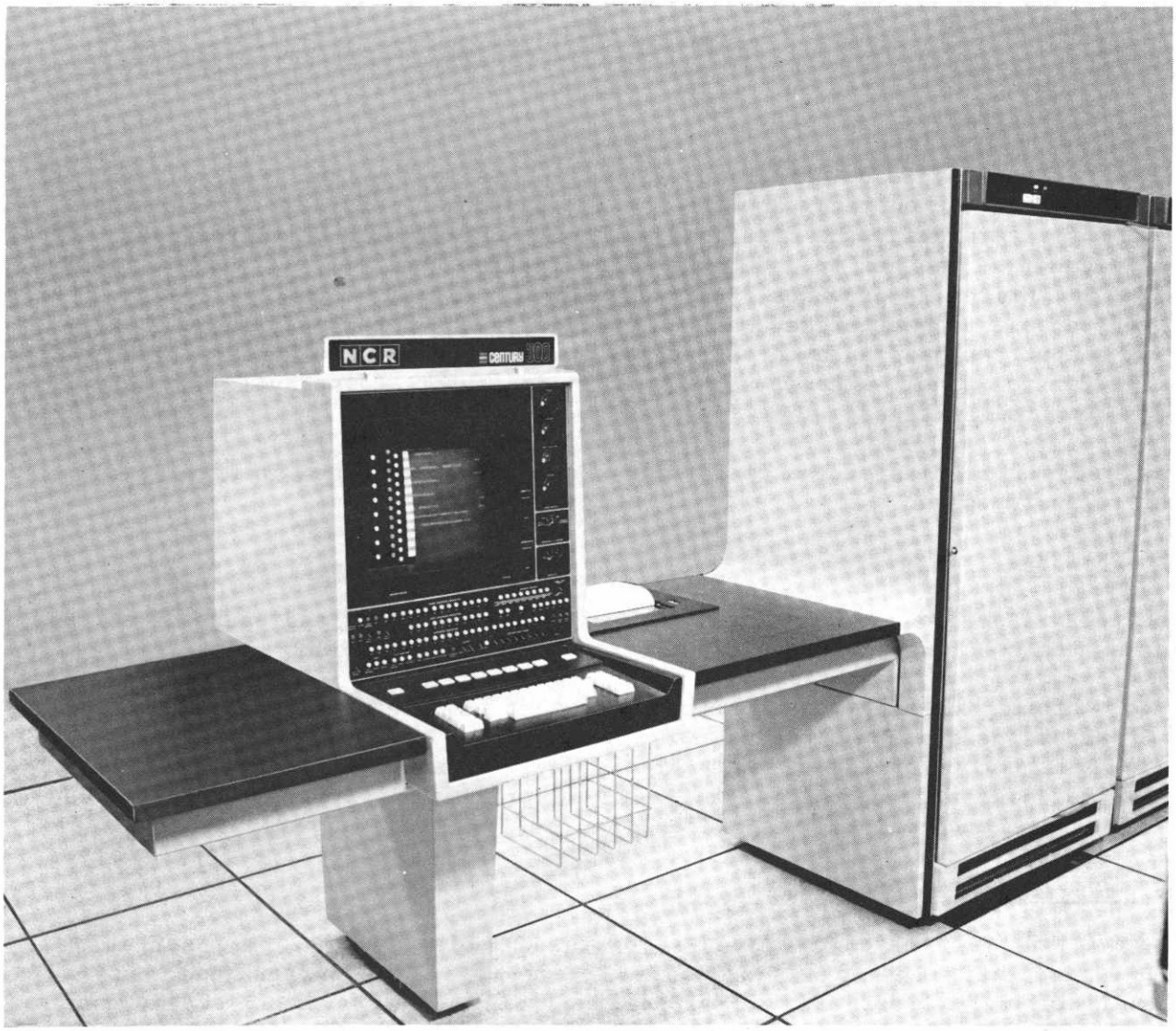
While the ALP is in the Halt state and the COMPUTE switch is pressed, the processor executes commands one at a time, commonly called single-stepping. The timer does not count during single-stepping. The timer resumes counting after leaving the Halt state, with the first "tic" (one millisecond count of the timer) occurring not less than one and not more than two milliseconds later.

NOTE

> The IOC and the ALP have independent access to memory; therefore, there exists a possibility that software establishes a new NA value immediately following a "tic" of the timer. After the IOC has incremented and compared the NA portion of the control word to the TA portion, it restores the incremented NA portion in the control word, destroying the value just established by software. To circumvent this problem, software stores the new NA value in the control word a second time, nine or more microseconds later.

OPERATOR'S CONSOLE

INTRODUCTION



The NCR Century 300 operator's console, comprising a CRT Display Unit, a keyboard, a control panel, and an I/O Writer, is the primary means of communication between the operator and the computer. To fully use the advanced NCR operating systems and to take advantage of the increased hardware capabilities, the operator must have a means to query the computer rapidly and efficiently. It is equally important that the computer convey to the operator as rapidly as possible answers to these queries, in order that the operator may make the decisions and judgements required of him.

Utilizing the operator's console, the operator can monitor the progress of current jobs, review status (pending, active, or terminated) of jobs in the system, review the allocation and availability of resources (memory, peripherals, etc.), display and respond to messages, and exercise control over the operation of the system by manually entering instructions and data via a control panel and/or a keyboard.

The following integrated peripherals and components are incorporated in the operator's console:

- Cathode Ray Tube (CRT) Display Unit -- displays system status, messages between the operator and the system, and other pertinent information. By interpreting the data displayed on a CRT Display Unit, the operator can make changes or additions in an instant.
- I/O Writer -- provides a hard copy of the CRT displays.
- Console typewriter keyboard -- provides means for manual input. The input can be displayed on the CRT, printed on the I/O Writer, or both.
- Control panel -- consists of various indicators, display lights, and control switches.

The individual units of the operator's console are described in more detail on the following pages.

I/O WRITER

The I/O Writer produces a printed copy of system messages and operator actions. The system's software uses the I/O Writer to print the following:

- Information-only messages (messages that require no operator response) from the system or the user.
- A hard copy of the current CRT display, if requested by the operator.
- Date the time at regular intervals (approximately every 15 minutes) as a reference point.

Physical Description

The I/O Writer, located to the right of the CRT Display Unit, is a serial, non-impact thermal printer. Printing is done by a single print head, consisting of a 7 x 5 dot matrix. By heating the selected elements of the matrix and bringing them into light contact with heat-sensitive paper, the character image is formed on the paper. The length of the print line is 80 characters. Functions included for page formatting are backspace, line feed, and carriage return, which may be initiated by pressing the appropriate key on the keyboard. Line feed and carriage return are initiated automatically when the printhead reaches the end of a line. The nominal printing rate of the I/O Writer is 30 characters per second.

Functional Description

- Command Operation

  Execution of an INOUT compand selects the I/O Writer and issues one of the following function codes:

- Input Permit
- Output
- Reset

Input/output operations through the I/O Writer require the transmission of two PAF characters -- trunk/position number and function.

Byte 1 of the PAF specifies the trunk and position number of the I/O Writer, The second PAF character specifies the desired function.

PERIPHERAL ADDRESS FIELD	
8 7 6 5 4 3 2 1	8 7 6 5 4 3 2 1
T T T P P P	F F

T = Trunk number (000 for the I/O Writer)
P = Position number (101 for the I/O Writer)
F = Function code 00 = Reset
01 = Input Permit
10 = Output

Only the two least significant bits of the function PAF character are used. The remaining bits are ignored.

The following table briefly describes the functions initiated by the function codes of the PAF.

FUNCTION CODES		
Code	**Name**	**Function**
XXXXXX00	Reset	Turns OFF the input permit flag and places the I/O Writer control in the idle mode. The processor does not store an S2 status character of Command-Initiated until the input permit flag is turned OFF. No S3 status character is sent to the processor.
XXXXXX01	Input Permit	Turns ON the input permit flag and places the I/O Writer control in the input mode. The processor does not store an S2 status character of Command-Initiated until the input permit flag is turned ON. No S3 status character is sent to the processor at this time.
XXXXXX10	Output	Places the I/O Writer control in the output mode. The processor does not store an S2 status character of Command-Initiated until the I/O Writer control has entered the output mode.

- Response

The response number selects the control word used in conjunction with a peripheral during an I/O operation. The I/O Writer response number is two, and it selects control word two at memory location 1040, which is reserved for the I/O Writer.

- Modes of Operation

The I/O Writer has three functional modes of operation: idle, input and output.

- Idle Mode

The idle mode is a neutral state from which the other two modes are entered. The I/O Writer is placed in the idle mode in one of three ways:

- Power turned on initially
- Termination of an input or output function
- Completion of a reset function

- Input Mode

The I/O Writer enters the input mode whenever it receives the input permit function code from the processor. The keyboard is assigned logically to the I/O Writer (rather than to the CRT, which is also serviced by the keyboard) and the I/O Writer-Keyboard Indicator light is turned ON. Data is received from the keyboard by the I/O Writer Control Unit, which then requests service from the processor to transfer the assembled character to memory. If additional data is received from the I/O Writer before completion of the data transfer by the IOC, a system overload occurs. Additional data from the I/O Writer cannot be accepted after a system overload. The program must reselect the I/O Writer and place it in the input mode before the transfer of additional data. Termination of the operation causes an S3 status character to be transmitted to the processor; the I/O Writer enters the idle mode. A latent error condition inhibits the transmission of the S3 status after termination.

- Output Mode

The I/O Writer enters the output mode whenever it receives the output function code from the processor. When in the output mode, the I/O Writer Control Unit resets the data register and requests service from the processor. The processor transfers a character to the data register. From the data register the character is transferred to the I/O Writer where it is either printed or used to initiate a non-print function (line feed, carriage return, etc.). When data transfer to the I/O Writer is completed, the data register is reset; this initiates another I/O request to the processor. The above procedure is repeated until termination of the operation. Termination causes an S3 character to be transmitted to the processor and the I/O Writer enters the idle mode. A latent error condition inhibits transmission of the S3 after termination. In the output mode the I/O Writer cannot cause a system overload.

NOTE

With the printhead positioned at the last character position of the line, if a print character is received, that character is printed, and the I/O Writer initiates a carriage return and line feed function. Any characters sent to the I/O Writer while the carriage (printhead) is returning are ignored and not printed.

If a carriage return character is received, regardless of the printhead's position, the IOC delays transmission of additional characters until the carriage return function is completed.

- Status Character

Three different status characters may be stored to reflect the result of a specific phase of an I/O operation. An S2 status character reflects the results of a selection attempt, an S3 status character reflects the results of the data transfer at termination, and if an error occurs in transmission and the S3 status character is inhibited by the IOC, an S4 status character is generated and stored in place of the S3.

The following table lists all of the status characters associated with the I/O Writer and a brief functional description of each.

INPUT/OUTPUT WRITER STATUS CHARACTERS

Status	Character	Condition	Indicates
			Condition during selection process
S2	00000010	Inoperative	I/O Writer is performing a function when a selection attempt is made; however, the reset function is accepted when the I/O Wrtier is in the input mode.
S2	01000000	Command Initiated	All operating conditions satisfied, PAF accepted.
			Condition occurring after selection
S3	00000000	Operation Complete	An end-of-message (EOM) was received during input and no errors or exception conditions occurred.
S3	11000000	Segment Complete	The NA character of the CW is equal to the TA character of the CW during input or output and last character on input was not end-of-message.
S3	00000010	Inoperative	I/O Writer becomes inoperative after selection but before normal termination (after loss of power to the I/O Writer, for example).
S3	00010000	System Overload	IOC did not respond to a request for service before the arrival of the next character at the register.
S4	10000001	Transmission Error	Error in transmission – parity error.

- Termination

Normal termination occurs when a processor terminate signal is received or an end-of-message (EOM) character is entered from the keyboard. If the termination is a result of a processor terminate signal, a Segment Complete S3 status character is stored; for EOM character termination, an Operation Complete S3 status character is stored.

Either the processor or the I/O Writer Control can detect an error condition. If the processor detects an error, it sends an error signal to the I/O Writer Control. The I/O Writer control turns off the input permit mode flag and places the writer in the idle mode; S3 status is not sent by the I/O Writer Control, in this case. If the I/O Writer Control detects the error, it turns off the input permit flag, places the writer in the idle mode, and sends an Inoperative S3 status character to the processor.

During an input operation, the EOM character is detected by the I/O Writer Control Unit. The EOM character is transmitted to the processor and the operation terminates. During an output operation, the EOM character (BELL character) is transmitted to the I/O Writer as a normal character without any special effect on the operation.

- Data Configuration

The data transmitted to the I/O Writer are either print characters or control characters. Print characters are those that cause a visible character image to be formed on the heat-sensitive paper. Control characters are those that cause some mechanical function to occur in the I/O Writer (for example, line feed, carriage return, etc.).

During an output operation the printed character set is the same as the NCR Century character set. Zero is represented as "Ø". During an input operation any character with bits 6 and 7 both true cannot be input.

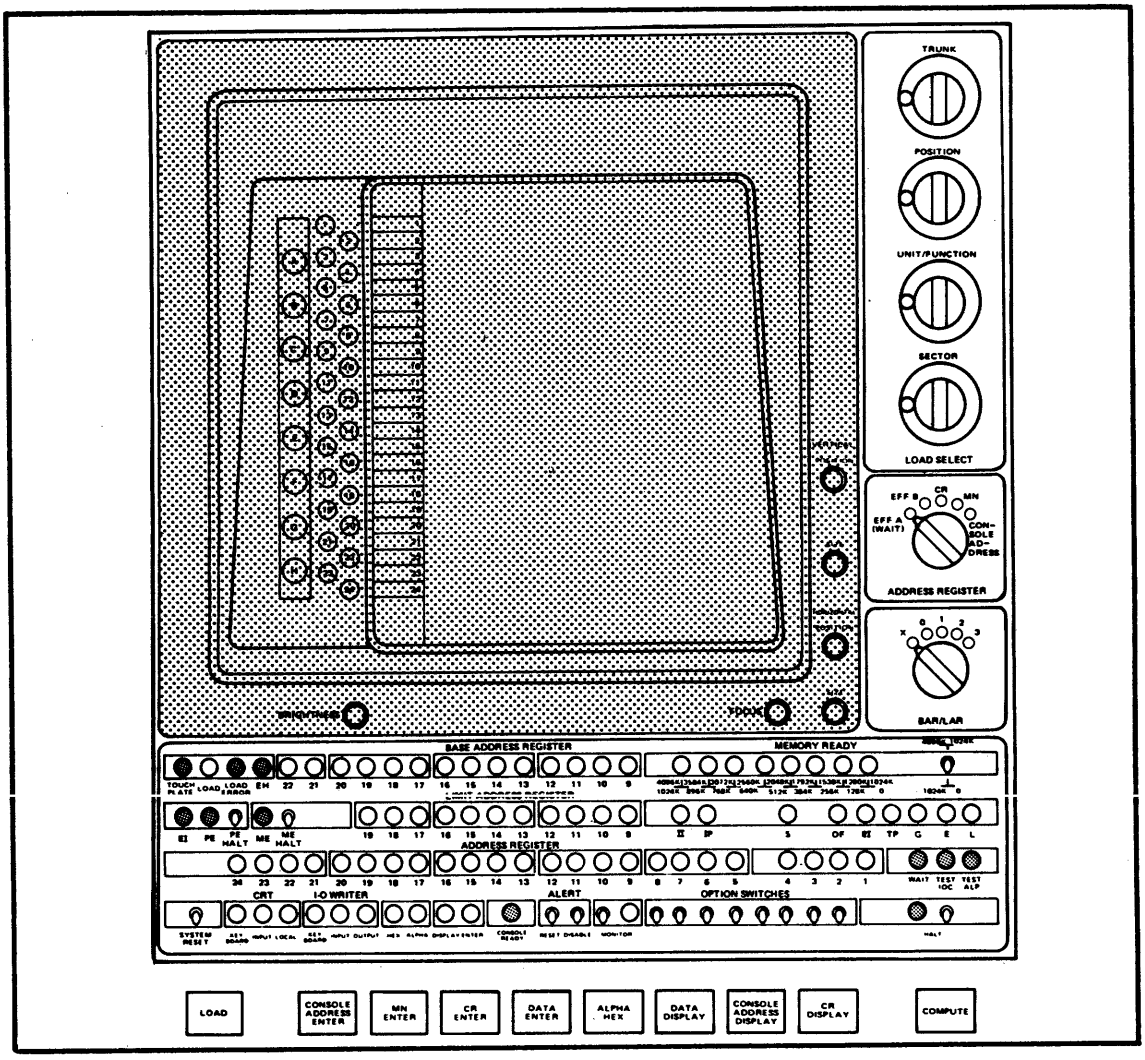
The following chart shows the printable characters of the I/O Writer.

I/O WRITER CHARACTER SET

Bits b_7 b_6 b_5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4 b_3 b_2 b_1 Row \ Col.	0	1	2	3	4	5	6	7
0 0 0 0 0	NUL	DLE	SP	0	@	P	`	p
0 0 0 1 1		DC1	!	1	A	Q	a	q
0 0 1 0 2		DC2	"	2	B	R	b	r
0 0 1 1 3		DC3	#	3	C	S	c	s
0 1 0 0 4		DC4	$	4	D	T	d	t
0 1 0 1 5			%	5	E	U	e	u
0 1 1 0 6			&	6	F	V	f	v
0 1 1 1 7			'	7	G	W	g	w
1 0 0 0 8	BS		(	8	H	X	h	x
1 0 0 1 9			)	9	I	Y	i	y
1 0 1 0 10	LF		*	:	J	Z	j	z
1 0 1 1 11			+	;	K	[	k	{
1 1 0 0 12			,	<	L	\	l	¦
1 1 0 1 13	CR		-	=	M	]	m	}
1 1 1 0 14			.	>	N	↑	n	~
1 1 1 1 15			/	?	O	←	o	DEL

Note: b_8 (not shown) = 0 for the characters shown above. The seven bit set conforms to the American Standard Code for Information Interchange (ASCII).

CONTROL PANEL



Physical Description

The control panel consists of various switches and indicator lights. Located on the panel above the I/O Writer-CRT keyboard are 10 pushbutton switches for initiating certain functions and entering or displaying control information necessary for the operation of the system. Arranged vertically to the right of the CRT are four rotary switches for establishing PAF characters during manual loading operations. Located below these are the Address Register Switch and the BAR/LAR Switch. Located below the CRT unit are additional control switches and indicator lights. The indicator lights are used for displaying the contents of certain registers, the memory configuration in use, and the processor status. The switches are used to place the processor in the halt state, to use the monitoring feature, and to exercise certain options available with the NCR Century 300.

For a complete description of the functions performed by the switches and

indicators on the Control Panel, refer to the NCR CENTURY OPERATORS INFORMATION MANUAL.

Operator Alert Indicator

The operator alert indicator is an audible alarm, sufficiently loud to be heard above the normal noise created by a data processing system. The function of the alarm is to alert the operator when a program stops or when a program requires operator intervention. The operator alert disable switch on the console provides the operator with a manual override of the alarm.

The alarm sounds when either of the following sets of conditions exist:

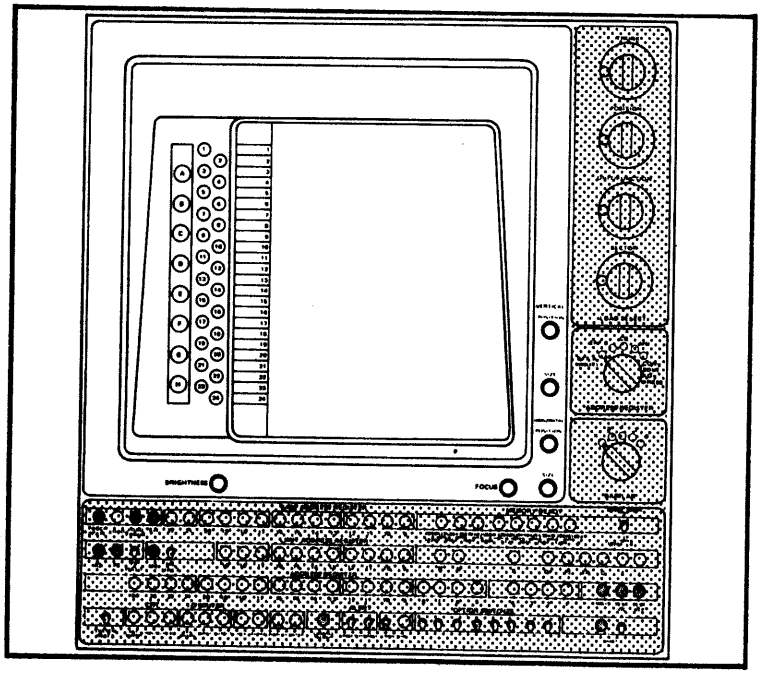
1. The processor power is on.
   The processor halt switch is off.
   The processor is not in the "test" state.
   The operator alert disable switch is off.
   The processor is in a wait and/or error halt state.

2. The processor power is on.
   The processor halt switch is off.
   The processor is not in a wait and/or error halt state.
   The operator alert disable switch is off.
   A special programmable character is output to the I/O Writer.

If either set of conditions exists, the operator alarm is activated. Once activated, the alarm continues to sound until the operator activates the reset switch.

As an option, an additional alarm may be used in parallel with the operator alert indicator. The optional alarm may be located up to 100 feet from the console.

CRT DISPLAY SYSTEM



The CRT Display System is the main device used by the operator to communicate with the computer. With greater flexibility and rapid response, the CRT Display System provides the operator with instantaneous access to program and system status information.

The CRT Display System functionally comprises two separate units: the Touchplate Switches and the CRT Display Unit. Each is described in more detail on the following pages.

Under control of the operating system, the CRT Display System is used to display system status, user messages, system messages, and system requests. The use of these displays and the CRT operating procedures are described in detail in the NCR CENTURY OPERATORS INFORMATION MANUAL.

TOUCHPLATE SWITCHES

Physical Description

The CRT Display Unit is controlled by 32 Touchplate Switches placed vertically on the left side of the Display Unit. The Control Panel has a "Touchplate" light to indicate when the touchplate switches are "live", i.e., the switches are selected for input. When the operator presses any one of the selected switches, the function assigned to that switch is initiated.

The touchplate switches are divided into two groups: 24 numeric switches aligned with the screen lines, and 8 alpha control switches immediately to the left of the line switches.

Functional Description

- Command Operation

  Execution of an INOUT command selects the Touchplate Switches and issues the function code which can be either RESET or INPUT PERMIT. I/O operations involving the Touchplate Switches require the transmission of two PAF characters -- trunk/position number and function. Byte 1 of the PAF specifies the trunk/position number and byte 2 specifies the function that the Touchplate Switches are to perform.

PERIPHERAL ADDRESS FIELD	
8 7 6 5 4 3 2 1	8 7 6 5 4 3 2 1
T T T P P P	0 0 0 0 F 0 0 F

T = Trunk number (000 for the Touchplate Switches)
P = Position number (000 for the Touchplate Switches)
F = Function Code 00001000 = Reset
00001001 = Input Permit

The following table explains the actions initiated by the Touchplate Switches function codes.

FUNCTION CODES		
Code	**Name**	**Function**
00001000	Reset	Turns OFF the input permit flag and places the Touchplate Switches in the idle mode. The Touchplate Indicator is turned OFF. The processor does not store an S2 status character of Command-Initiated until the input permit flag is turned OFF. No S3 status character is sent to the processor.
00001001	Input Permit	Turns On the input permit flag and places the Touchplate Switches in the input mode. The processor does not store an S2 status character of Command-Initiated until the input flag is turned ON. The Touchplate Select Indicator is turned ON. No S3 Status character is sent to the processor.

- Response

The response number for the Touchplate Switches is three. The response number selects the control word used in conjunction with the peripheral during an I/O operation. Response number three selects Control Word three at address 1048, which is permanently assigned to the Touchplate Switches.

- Modes of Operation

The Touchplate Switches have two functional modes of operation: idle and input permit.

- Idle Mode

The idle mode is a neutral state. Whenever the input permit flag is OFF the touchplates are in the idle mode. The touchplate switches are placed in the idle mode in one of three ways:

- Power turned on initially
- Completion of a RESET function
- Releasing a pressed Touchplate Switch when in the input mode

- Input Permit Mode

The Touchplate Switch Control Unit is placed in the input permit mode whenever it receives the input function code from the processor. By pressing and then releasing a Touchplate Switch sends one character of data to the processor, resets the input permit flag, and turns OFF the Touchplate Indicator. To input additional data, the above sequence is repeated.

The character sent to the processor designates the Touchplate Switch that was released. The 24 numeric switches are designated binarily by the five least significant bits; bits 6 through 8 are 0.

The 8 alpha switches are designated binarily by the three least significant bits. Bit 6 is ON to distinguish the control switches from the line switches; bits 4, 5, 7 and 8 are 0.

SWITCH DESIGNATION			
CONTROL SWITCHES		LINE SWITCHES	
Bit Configuration	Switch Designation	Bit Configuration	Switch Designation
0010 0000	A	0000 0000	1
0010 0001	B	0000 0001	2
0010 0010	C	0000 0010	3
0010 0011	D	•	•
0010 0100	E	•	•
0010 0101	F	•	•
0010 0110	G		
0010 0111	H	0001 0101	22
		0001 0110	23
		0001 0111	24

- Termination

  When the transfer of the data character is complete, the Touchplate Switch control unit sends an Operation Complete S3 status character to the processor to terminate the operation. The Touchplate Switches are deselected and placed in the idle mode.

CRT DISPLAY UNIT

Physical Description

The CRT Display Unit is a vertical alphanumeric display unit with a 7 x 8.5 inches viewing screen. A total of 960 characters may be displayed with 40 characters to a line, and 24 lines to a page. Each character is formed by displaying the required portions of a 35-dot five-by-seven matrix. The CRT Display Unit can display 82 characters out of a possible 128 character set (ASCII). Any character that is not part of the CRT 82-character code set is displayed as the full 35-dot character which forms a rectangle. The memory configuration of the character is not affected.

The display on the CRT screen is adjusted by a set of switches on the display unit.

The vertical position control moves the entire display up or down on the viewing screen. The vertical size control moves the display lines vertically closer to each other or farther apart.

The horizontal position control moves the entire display either to the left or the right on the viewing screen. The horizontal size control moves the display lines horizontally closer to each other or farther apart.

The focus control adjusts the focus of the display on the viewing screen.

The brightness control adjusts the brightness of the display to suit personal preferences and to compensate for lighting conditions.

Functional Description

- Command Operation

Execution of the INOUT command selects the CRT Display Unit and issues one of the following function codes:

- Reset
- Input-Local
- Output
- Input-Transmit

I/O operations involving the CRT Display Unit require either two or five PAF characters. Both input operations, local and transmit, require the transmission of five PAF characters. The reset and output functions require two PAF characters.

The first two PAF characters are the same for all functions -- Trunk/position number and the Function Code.

PERIPHERAL ADDRESS FIELD - FIRST AND SECOND BYTE	
8 7 6 5 4 3 2 1	8 7 6 5 4 3 2 1
T T T P P P	F F F

T = Trunk number (000 for the CRT)
P = Position number (000 for the CRT)
F = Function code 00000000 = Reset
00000001 = Input-Local
00000010 = Output
00000101 = Input-Transmit

The input functions, Input-Local and Input-Transmit, require three additional PAF characters to specify the location of the cursor.

PERIPHERAL ADDRESS FIELD- THIRD THROUGH FIFTH BYTE		
8 7 6 5 4 3 2 1	8 7 6 5 4 3 2 1	8 7 6 5 4 3 2 1
0 0 0 1 1 0 1 0	0 0 0 L L L L L	0 0 C C C C C C

00011010 = Hexadecimal character 1A, the Jump Cursor character
L = Line location of the cursor
C = Character location of the cursor

The 5 least significant bits (L) in the 4th PAF character indicate the line location (0 through 23 with 0 specifying line 1) of the cursor.

To indicate the character position of the cursor, the fifth PAF character uses the least significant six bits (C) to count binarily from 0 through 39, for a total of 40 horizontal characters on the viewing screen of the CRT. Bits 7 and 8 of the PAF character are 0.

The following table briefly describes the functions initiated by the function codes of the PAF.

FUNCTION CODES		
Code	**Name**	**Function**
00000000	Reset	Turns OFF the Input-Local flag and places the CRT unit in the idle mode. The CRT-Input and CRT-Local indicators are turned OFF. The processor does not store an S2 status character of Command-Initiated until the Input-Local flag is turned OFF. No S3 status character is sent to the processor.
00000001	Input-Local	Turns ON the Input-Local flag and places the CRT unit in the input mode. The processor does not store an S2 status character of Command-Initiated until the Input-Local flag is turned ON. The CRT-Input and CRT-Local indicators are turned ON. The keyboard is assigned logically to the CRT unit and the CRT-Keyboard indicator is turned ON. The processor does not receive an S3 status character at this time.
00000010	Output	Turns ON the output flag and places the CRT unit in the output mode. The processor does not store an S2 status character of Command-Initiated until the output flag is turned ON. No S3 status character is sent to the processor at this time.
00000101	Input-Transmit	Turns ON the Input-Transmit flag and places the CRT unit in the Input-Transmit mode. The processor does not store an S2 status character of Command-Initiated until the Input-Transmit flag is turned ON. The CRT-Local indicator is turned OFF. The processor does not receive an S3 status character at this time.

- Response

The CRT Display Unit has two response numbers and uses two control words: one for the input mode, one for the output mode.

In the input mode the CRT Display Unit responds with the number 1 and uses control word 1 at memory location 1032 during the I/O operations. In the output mode the CRT Display Unit responds with the number 4 and uses control word 4 at memory location 1056 during the I/O operations.

By assigning two response numbers and two control words to the CRT Display Unit, two-way simultaneity is achieved; the unit can output information at the same time that the operator is inputting information.

- Modes of Operation

The CRT Display Unit has four modes of operation: Idle, Input-Local, Output, and Input-Transmit.

  - Idle Mode

The idle mode is the neutral state of the CRT Display Unit. In the idle mode, the input flag is off. The idle mode is entered in one of two ways:

- Power turned on initially
- Completion of a RESET function

- Input-Local Mode

The CRT Display Unit enters the Input-Local mode when it receives the input-local function code from the processor. The Third, Fourth, and Fifth PAF characters position the cursor to the line and character position in that line where the local input by the operator is to begin. Software determines the location of the cursor prior to the execution of the INOUT command.

The Input-Local mode of operation consists of two internal stages: the input stage and the transmission stage.

During the input stage, all characters on the keyboard are entered, one at a time, into a register in the I/O Control. From the I/O Control they are transmitted to a one-character buffer in the CRT Display Unit, displayed on the CRT and then entered into the CRT cyclic memory.

The beginning of the local input field is marked by inserting a flag into each character position that is input; therefore, the operator must not move the cursor during local input, except within the local field defined by software.

During the transmission stage, which is entered by depression of the XMIT (Transmit) key on the keyboard, the cursor moves automatically to the home position. From that position the cursor begins a search until it finds the beginning of the local field. The CRT Unit requests service from the processor and the transfer of data from the CRT cyclic memory to the processor begins. When the data in the CRT memory has been transferred, the operation terminates and an S3 status characteris sent to the processor.

- Output Mode

The CRT Unit is placed in the output mode when it receives an output function code from the processor. In the output mode, the first three bytes of data transmitted are the Jump Cursor character, the line position and the relative character position of the cursor within that line. The remaining bytes of data are transmitted to the CRT cyclic memory and displayed on the screen. When the output data has been transferred to the CRT memory, the operation terminates, and an S3 status character is sent to the processor.

NOTE

During the output mode of operation, if the data transmitted overlaps into a Local-Input character field, the flag associated with each overlapped character in the Local-Input field is erased and the ability to locate the beginning of the local field is lost.

- Input-Transmit Mode

  The CRT Unit enters the Input-Transmit mode when it receives the input-transmit function code from the processor. The third, fourth, and fifth PAF characters position the cursor to the line and the character position in that line where the transmission of data is to start. The CRT Unit requests service from the processor and the transfer of data starts from the position marked by the cursor and continues till termination. An S3 status character is sent to the processor when the operation terminates.

- Status Character Transmission

Status of the CRT Display System is indicated at three different times during the operation by transmission of a status character to the processor. Three distinct status characters may be stored by the processor, each at a specific time indicating a specific condition: an S2 during the selection process, an S3 at the termination of an input or output function, or an S4 if an error occurred during the transmission of data and the transmission of an S3 is inhibited.

In most cases if the CRT Unit is performing a function and an attempt is made to select it for another function, the selection will be performed and an S2 of command-initiated is stored by the processor. However, the combinations of functions shown in the following table prohibit selection and cause an S2 of busy to be stored by the processor.

Function In Process	Function In Process Of Selecting	S2 Status Stored
Input-Transmit	Reset	10000000 Busy
Input-Transmit	Input-Local	10000000 Busy
Input-Transmit	Input-Transmit	10000000 Busy
Input-Local	Input-Local	10000000 Busy
Input-Local	Input-Transmit	10000000 Busy
Output	Output	10000000 Busy

If an attempt is made to select the CRT Unit when it is in the input stage of the Input-Local mode of operation, the selection is completed; if the CRT Unit is in the transmission stage, the selection is not completed and an S2 Busy status is sent to the processor.

If the CRT Display Unit is selected for an output function, while it is in the Input-Local mode to permit the operator to enter data through the keyboard, the Input-Local mode is temporarily suspended until the completion of the output function; control is then returned to the Input-Local function. During the time when the Input-Local function is suspended, the operator can continue to input data through the keyboard. Due to the speed of the operation, the Output function is usually completed and control returned to the Input-Local mode before the next character on the keyboard is entered. If, however, a character on the keyboard is entered before control is returned to the Input-Local function, a System Overload occurs, the operation terminates and an S3 status character of System Overload is sent to the processor.

When any function is terminated, an S3 status character is sent to the processor to indicate the status of the termination. The following illustration shows the possible S3 status characters sent to the processor and a brief functional description of each.

S3 STATUS CHARACTERS

Bit Configuration	Name	Description
0000 0000	Operation Complete	Indicates that an End of Text (ETX) character has been received on an input operation and no errors or exceptions exist.
1100 0000	Segment Complete	Indicates that NA = TA in the processor during an input or output operation and the last character transmitted on input was not an ETX character.
0001 0000	System Overload	Indicates that I/O Control did not respond to a request for service before the next character was input to the register. This S3 status character is indicative of loss of data.
0000 0001	Special	Indicates that, while in the Input-Local mode, the local field was not established before the unit was selected for an output function and the input function was suspended; when control is returned to the Input-Local mode, the local field cannot be established, since it was not started, the cursor is moved to the HOME position, the Input-Local function is terminated and an S3 status of 01 is sent to the processor.
0000 0010	Inoperative	Indicates that the CRT entered the "Not-ready" state during an I/O operation. The not-ready condition may be either long-term or short-term. The long-term not-ready condition usually requires manual intervention to restore the CRT to the ready state. The short-term not-ready condition is self-correcting. The system software, after the INOPERATIVE S3 status character has been detected, initiates a re-try of the same operation. If a second INOPERATIVE S3 is detected, software assumes the condition to be the long-term type and no more re-tries are initiated. This S3 status character is also indicative of an out-of-range cursor position character sent to the CRT that caused the cursor to be positioned off-screen.

- Termination

  Normal termination occurs when the terminate signal is received from the processor as a result of NA = TA, or when an End-of-Text (ETX) character is detected. The processor terminate signal (NA = TA) causes the CRT to send a Segment Complete S3 status character to the processor. The detection of an ETX character causes the CRT to send an Operation Complete S3 status character to the processor. The detection of an ETX character causes the operation to terminate on input only. During an output operation, the ETX character is transmitted to the CRT Unit as a display character.

Character Set

The CRT Display Unit recognizes 82 characters out of the NCR Century Code Set of 128 characters. Any character that is not recognized by the CRT Unit is displayed as a full 35-dot box. The character is retained in CRT memory in the correct bit configuration and can be transmitted to the processor in the correct form.

The following illustration is a chart of the CRT Character Set.

CRT CHARACTER SET

b_7 b_6 b_5 → / Bits					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4 ↓	b_3 ↓	b_2 ↓	b_1 ↓	Col. / Row →	0	1	2	3	4	5		
0	0	0	0	0	NUL		SP	0	@	P		
0	0	0	1	1		Line Clear	!	1	A	Q		
0	0	1	0	2		FS	"	2	B	R		
0	0	1	1	3	ETX	RLF	#	3	C	S		
0	1	0	0	4		HOME	$	4	D	T		
0	1	0	1	5			%	5	E	U		
0	1	1	0	6			&	6	F	V		
0	1	1	1	7	BEL		'	7	G	W		
1	0	0	0	8	BS		(	8	H	X		
1	0	0	1	9	TAB		)	9	I	Y		
1	0	1	0	10(A)	LF	SUB	*	:	J	Z		
1	0	1	1	11(B)	Tab Set	ESC	+	;	K	[		
1	1	0	0	12(C)	FF		,	<	L	\		
1	1	0	1	13(D)	CR	GS	-	=	M	]		
1	1	1	0	14(E)		RS	.	>	N	↑		
1	1	1	1	15(F)		US	/	?	O	←		

In addition to the characters that can be displayed on the CRT screen, there are control and special characters used in the operation of the CRT Display Unit. Some of these special characters are stored in the CRT memory, while others perform control functions during the operation and are not stored in the cyclic memory of the CRT Unit.

The following chart lists the control characters, their bit configuration as two hexadecimal characters and a brief functional description.

CONTROL AND SPECIAL CHARACTERS

Character	Hex Configuration	Description
NUL	00	Does not cause cursor to move; not stored in the CRT memory; not displayed.
ETX	03	End of Text – control character; stored in the CRT memory; transmission is halted after this character; displayed as X.
BEL	07	Bell – control character; in input-local, displayed and stored in the CRT memory as 35-dot box; no alarm is sounded. When received from MSU in OUTPUT, causes an audible tone of 240 Hz for 1.5 to 2.5 seconds but is not stored or displayed.
BS	08	Backspace – control character; not stored in CRT memory. Backspace cursor one character. When cursor is on left edge of page, BS causes it to reappear at the right edge of same line.
TAB	09	Tabulate – control character; not stored in CRT memory. Causes cursor to move forward to the next tab stop location. If no tab stop is found in a line, the cursor moves to the left edge of the next line.
LF	0A	Line Feed – control character; not stored in CRT memory. Moves cursor one line down; when the cursor is in the bottom line, LF causes it to appear in the top line.
TAB SET	0B	Set tabulation – control character; not stored in CRT memory. Causes a tab stop flag to be entered at the cursor horizontal location in all lines.
FF	0C	Form Feed – control character; not stored in CRT memory. Clears entire CRT memory, including tab stop flags. Cursor is positioned at top, leftmost position.
CR	0D	Carriage Return – control character; stored in the CRT memory. Displayed as $\overline{\nabla}$. Returns cursor to leftmost position, next line down.

CONTROL AND SPECIAL CHARACTERS		
Character	**Hex Configuration**	**Description**
Line Clear	11	Line Clear – control character; not stored in CRT memory. Erases all data in the line except tab flags. Data will be erased from the cursor position (including the cursor position) up to and including the last character in the line.
FS	12	Forward space – control character; not stored in the CRT memory. Moves cursor one position to the right. If the cursor is at the right edge of the page, FS causes it to reappear at the left edge down shifted one line. If the cursor is located in last position of bottom line, FS causes it to reappear in Home position.
RLF	13	Reverse Line Feed – control character; not stored in CRT memory. Causes the cursor to be moved one line up. When the cursor is in the top line, RLF causes it to reappear in the bottom line.
HOME	14	Home – control character; not stored in CRT memory. Causes cursor to be moved to Home (upper left) position.
SUB	1A	Jump Cursor – control character; not stored in CRT memory. The CRT in OUTPUT mode is alerted to a sequence of SUB plus two following characters. The first character is line address to which the cursor is moved. The second character is the "character" position to which the cursor is moved.
ESC	1B	Report Cursor – control character; not stored in the CRT memory:*
GS	1D	Cursor control character; stored in CRT memory on receipt from MSU. Displayed as △. Cannot be stored or generated from Keyboard. Has no function in system at present time.
RS	1E	Cursor control character; stored in CRT memory on receipt from MSU. Displayed as ◁. Cannot be stored or generated from Keyboard. Has no function in system at present time.
US	1F	Cursor control character; stored in CRT memory on receipt from MSU. Displayed as ▷. Cannot be stored or generated from Keyboard. Has no function in system at present time.
CURSOR		In an empty or nulled position is displayed as ◇. In an occupied position, that character will blink. It is non-destructive.

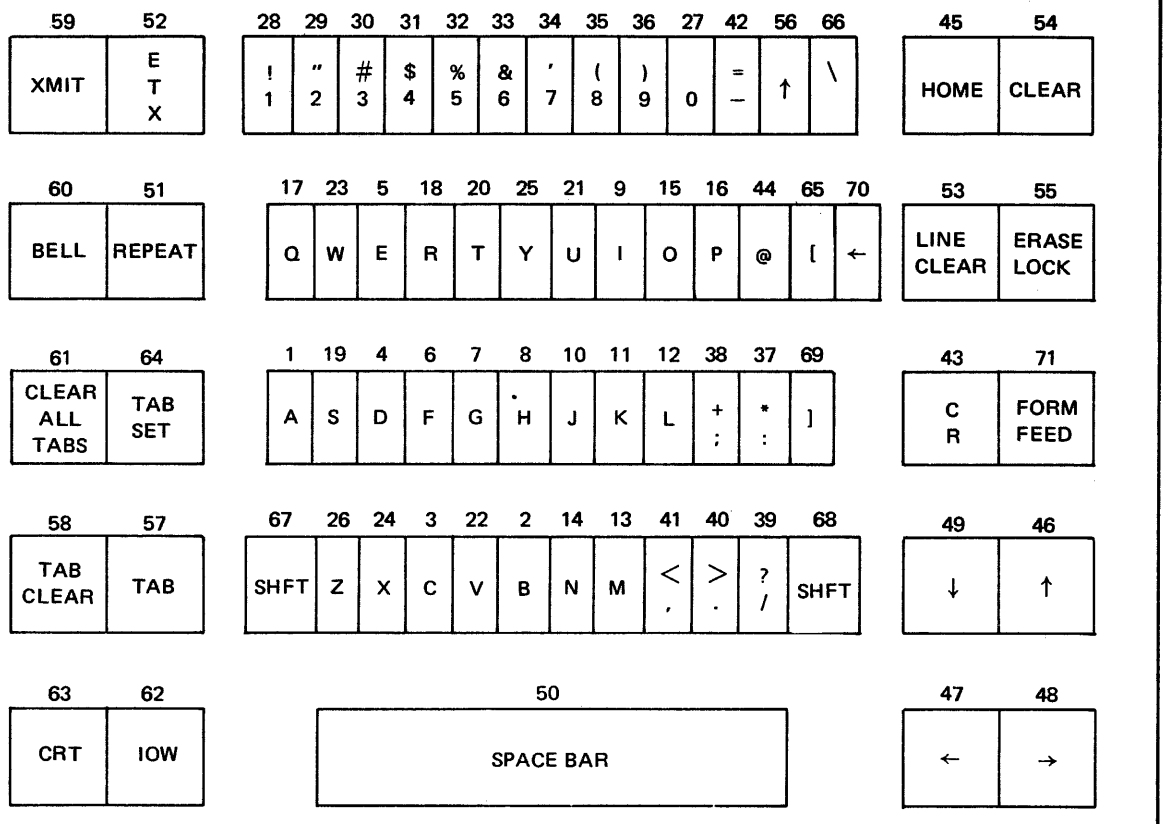
* When the Report Cursor character received in the data stream in OUTPUT causes the function to suspend activity, two characters are sent to MSU, then OUTPUT resumes activity.

KEYBOARD

The keyboard of the operator's console is shared by the I/O Writer and the CRT Display Unit. In addition to the alpha, numeric and special characters shown in the I/O Writer Character Set, the keyboard has certain control keys used in conjunction with the I/O Writer and the CRT Display Unit.

The following illustration shows the keyboard configuration and key top reference designation. Each key is also referenced by a number above the key. The charts that follow the keyboard illustration contain the ASCII and the 8-bit binary codes for each key on the keyboard, the corresponding character printed on the I/O Writer and displayed on the CRT Display Unit. Both upper and lower shifts are illustrated.

KEYBOARD CONFIGURATION AND KEY TOP DESIGNATORS



KEYBOARD – CRT – I/O WRITER CHARACTER SET – LOWER SHIFT				
Key	ASCII	Binary	CRT Displays	I/O Writer Prints
1	A	0100 0001	A	A
2	B	0100 0010	B	B
3	C	0100 0011	C	C
4	D	0100 0100	D	D
5	E	0100 0101	E	E
6	F	0100 0110	F	F
7	G	0100 0111	G	G
8	H	0100 1000	H	H
9	I	0100 1001	I	I
10	J	0100 1010	J	J
11	K	0100 1011	K	K
12	L	0100 1100	L	L
13	M	0100 1101	M	M
14	N	0100 1110	N	N
15	O	0100 1111	O	O
16	P	0101 0000	P	P
17	Q	0101 0001	Q	Q
18	R	0101 0010	R	R
19	S	0101 0011	S	S
20	T	0101 0100	T	T
21	U	0101 0101	U	U
22	V	0101 0110	V	V
23	W	0101 0111	W	W
24	X	0101 1000	X	X
25	Y	0101 1001	Y	Y
26	Z	0101 1010	Z	Z
27	0	0011 0000	0	0
28	1	0011 0001	1	1
29	2	0011 0010	2	2
30	3	0011 0011	3	3
31	4	0011 0100	4	4
32	5	0011 0101	5	5
33	6	0011 0110	6	6
34	7	0011 0111	7	7
35	8	0011 1000	8	8
36	9	0011 1001	9	9
37	:	0011 1010	:	:
38	;	0011 1011	;	;
39	/	0010 1111	/	/
40	.	0010 1110	.	.
41	,	0010 1100	,	,
42	-	0010 1101	-	-
43	CR	0000 1101	▽	(Returns Carriage)
44	@	0100 0000	@	@
45	DC4(HOME)	0001 0100	(Home Function)	
46	DC3(RLF)	0001 0011	(RLF Function)	
47	BS	0000 1000	(Backspace Cursor)	(Backspaces)
48	DC2(FS)	0001 0010	(Forward Space Cursor)	
49	LF	0000 1010	(Feeds 1 Line)	(Feeds 1 Line)
50	SP	0010 0000	(Spaces 1 Position)	(Spaces 1 Position)
51			(Repeat Function)	
52	ETX	0000 0011	⧖	
53	DC1 (Line Clear)	0001 0001	(Line Clear Function)	
54			(Clear Function)	
55			(Erase Lock Function – See Note 1)	
56	^	0101 1110	↑	↑
57		0000 1001	(Tab Function)	
58			(Clear Tab Function)	
59			(Transmit Function)	
60	BEL	0000 0111	(Bell Function)	
61			(Clear All Tabs Function)	
62			(See Note 2)	
63			(See Note 3)	
64		0000 1011	(Tab Set Function)	
65	[	0101 1011	[	[
66	\	0101 1100	\	\
67			(See Note 4)	
68			(See Note 4)	
69	]	0101 1101	]	]
70	-	0101 1111	←	←
71		0000 1100	(Form Feed Function)	

KEYBOARD – CRT – I/O WRITER CHARACTER SET – UPPER SHIFT

Key	ASCII	Binary	CRT Displays	I/O Writer Prints
1	A	0100 0001	A	A
2	B	0100 0010	B	B
3	C	0100 0011	C	C
4	D	0100 0100	D	D
5	E	0100 0101	E	E
6	F	0100 0110	F	F
7	G	0100 0111	G	G
8	H	0100 1000	H	H
9	I	0100 1001	I	I
10	J	0100 1010	J	J
11	K	0100 1011	K	K
12	L	0100 1100	L	L
13	M	0100 1101	M	M
14	N	0100 1110	N	N
15	O	0100 1111	O	O
16	P	0101 0000	P	P
17	Q	0101 0001	Q	Q
18	R	0101 0010	R	R
19	S	0101 0011	S	S
20	T	0101 0100	T	T
21	U	0101 0101	U	U
22	V	0101 0110	V	V
23	W	0101 0111	S	S
24	X	0101 1000	X	X
25	Y	0101 1001	Y	Y
26	Z	0101 1010	Z	Z
27	0	0011 0000	0	0
28	!	0010 0001	!	!
29	"	0010 0010	"	"
30	#	0010 0011	#	#
31	$	0010 0100	$	$
32	%	0010 0101	%	%
33	&	0010 0110	&	&
34	'	0010 0111	'	'
35	(	0010 1000	(	(
36	)	0010 1001	)	)
37	*	0010 1010	*	*
39	+	0010 1011	+	+
39	?	0011 1111	?	?
40	>	0011 1110	>	>
41	<	0011 1100	<	<
42	=	0011 1101	=	=
43	CR	0000 1101	▽	(Returns Carriage)
44	@	0100 0000	@	@
45	DC4(HOME)	0001 0100	(Home Function)	
46	DC3(RLF)	0001 0011	(RLF Function)	
47	BS	0000 1000	(Backspaces Cursor)	(Backspaces)
48	DC2(FS)	0001 0010	(Forward Spaces Cursor)	
49	LF	0000 1010	(Feeds 1 Line)	(Feeds 1 Line)
50	SP	0010 0000	(Spaces 1 Position)	(Spaces 1 Position)
51			(Repeat Function)	
52	ETX	0000 0011	△	
53	DC1(Line Clear)	0001 0001	(Line Clear Function)	
54			(Clear Function)	
55			(Erase Lock Function – See Note 1)	
56	^	0101 1110	↑	↑
57		0000 1011	(Tab Set Function)	
58			(Clear Tab Function)	
59			(Transmit Function)	
60	BEL	0000 0111	(Bell Function)	
61			(Clear All Tabs Function)	
62			(See Note 2)	
63			(See Note 3)	
64		0000 1011	(Tab Set Function)	
65	[	0101 1011	[	[
66	\	0101 1100	\	\
67			(See Note 4)	
68			(See Note 4)	
69	]	0101 1101	]	]
70	-	0101 1111	←	←
71		0000 1100	(Form Feed Function)	

Note 1: Must be depressed along with Line Clear, Clear, or Form Feed to activate those functions.
Note 2: Function, connects Keyboard to IOW.
Note 3: Function, connects Keyboard to CRT.
Note 4: Shift, when depressed with any other key, produces upper case code or upper case function.

Some of the keys, explained in the previous chart, do not cause the I/O Writer to print nor are they displayed on the CRT Display Unit. These special keys perform certain control functions associated with data input and output. The following illustration lists the special keys and gives a brief functional description of each key.

SPECIAL KEY FUNCTIONS

#Of Key	Name Of Key	Description
59	XMIT	Transmit – Places the CRT Display Unit in the INPUT-TRANSMIT mode.
51	REPEAT	Repeat – When Repeat key is depressed along with any other key except XMIT, TAB CLEAR, or CLEAR, that key will be repeated at a rate of about 15 Hz. Depressed in conjunction with XMIT, TAB CLEAR, or CLEAR, Repeat has no effect.
63	CRT	Connects the keyboard logically to the CRT Display Unit.
62	IOW	Connects the keyboard logically to the I/O Writer.
53	Line Clear	Erases all data in the line (except tab flags) from cursor position to the end of the line. Erase Lock must be depressed at the same time as the Line Clear key. Cursor positioned at next line, leftmost position.
54	CLEAR	Erases all data on the screen, except the tab stop flags. Clear will not operate unless Erase Lock key is depressed at same time.
61	CLEAR ALL TABS	Erases all tab stops in all lines.
58	TAB CLEAR	Erases tab stops at cursor horizontal location in all lines.

NCR CENTURY 300 SPECIFICATIONS

PHYSICAL SPECIFICATIONS

PHYSICAL SPECIFICATIONS				
Characteristic	Specification			
	Console	IOC	ALP	Memory*
Power Requirements	Powered by the IOC	3-phase 5-wire 120/208V 60 Hz	3-phase 5-wire 120/208V 60 Hz	3-phase 5-wire 120/208V 60 Hz
KVA	–	4.5	3.5	2.9
Current by Leg	–	1 = 16A	1 = 13A	1 = 14A
	–	2 = 18A	2 = 10A	2 = 14A
	–	3 = 16A	3 = 8A	3 = 14A
Heat Dissipation	–	13,000 BTU	9,550 BTU	7,700 BTU
Dimensions				
Height	48 in.	66 in.	66 in.	66 in.
Width	67 in.	32 in.	32 in.	32 in.
Depth	36 in.	27 in.	27 in.	27 in.
Weight	400 lbs.	928 lbs.	965 lbs.	850 lbs.
Service Clearance**				
Rear	–	3 ft.	3 ft.	3 ft.
Front	–	3 ft.	3 ft.	3 ft.
Left Side	–	–	–	–
Right Side	–	–	3 ft.	–

* The specifications listed are for a 256K MSU.
** The service clearances listed are nominal clearances required for opening doors and removing panels of the equipment for necessary servicing.

ENVIRONMENTAL SPECIFICATIONS

The required environmental conditions for the NCR Century 300 Processor are as shown in the following table.

OPERATING LIMITS	
Temperature	68°F to 78°F Dry Bulb
Humidity	40% to 60% Relative
Altitude	7000 Feet Maximum

NOTE

The NCR Century 300 System must be installed on a raised floor.